A SOLID STATE PULSE MODULATED RADIOSONDE

by

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THESIS

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ABSTRACT

This thesis is concerned with the design and construction of a radiosonde utilizing solid state devices and state-of-the-art techniques. The radiosonde is designed with the idea of obtaining data at a ground station in digital form and transmitting this data direct to Weather Central via high speed data links. Pulse modulation is utilized to transmit the data from the radiosonde. The multiplexer (time multiplexing is utilized) is designed using MOS micro technology and a breadboarded simulation is accomplished using discrete MOS integrated circuits. A computer simulation of the actual multiplexer design is performed. The modulator and transmitter are of complete solid state design. Extensive testing of the overall system indicated satisfactory results and show a substantial improvement over the present radiosonde. Modification of ground receiving systems to facilitate proper reception of information from the radiosonde is also discussed.

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TABLE OF SYMBOLS AND ABBREVIATIONS

C	Capacitance
CAD	Computer Aided Design
f	Frequency
GVPRF	Gated Variable Pulse Repetition Frequency
H	Logic High
Hz	Hertz
I	Electrical Current
IC	Integrated Circuit
L	Logic Low
LSI	Large Scale Integration
mb	Millibar
MHz	MegaHertz
MOS	Metal Oxide Silicon
OSC	Oscillator
PRF	Pulse Repetition Frequency
R	Resistance
RF	Radio Frequency
SYNC	Synchronization
S/R	Shift Register
V	Volts
VCM	Voltage Controlled Multivibrator
VCO	Voltage Controlled Oscillator
XTAL	Crystal

°C	Degrees Centigrade
Δ	Incremental Quantity
Ω	Ohms
usec	Microseconds

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I. INTRODUCTION

Daily weather forecasting is accomplished through data obtained from radiosondes. The radiosondes are carried aloft by balloons and, during ascent, transmit pressure, temperature, and humidity data to a ground station. Two types of radiosondes are used; the AN/AMT-4 which operates at a frequency of 1680 MHz, and the AN/AMT-11 which operates at a frequency of 403 MHz. Both systems have vacuum tube modulators and transmitters and a Baroswitch [Ref. 1] which time multiplexes the humidity, temperature, and high or low reference data. Data is recorded at the terminal installations on charts and after interpretation and encoding is sent to a central facility. Information collected by the central facility is utilized in preparing daily weather forecasts. During data interpretation and encoding human errors are introduced. In addition, sensor inaccuracy is also a large contributor of error.

In order to improve system accuracy and reliability it would be desirable to eliminate any data reduction or interpretation at the ground station prior to transmission to the central facility. This could be accomplished easily be recording the data directly in digital form compatible with the computer format at Weather Central. The data could be transmitted over high speed digital links to the computer for final interpretation. Fig. 1 depicts this situation.

Another desirable feature would be an increase in the data rate and a capability to measure other atmospheric constituents such as ozone, etc. Corbeille [Ref. 2] concluded that "If accurate data

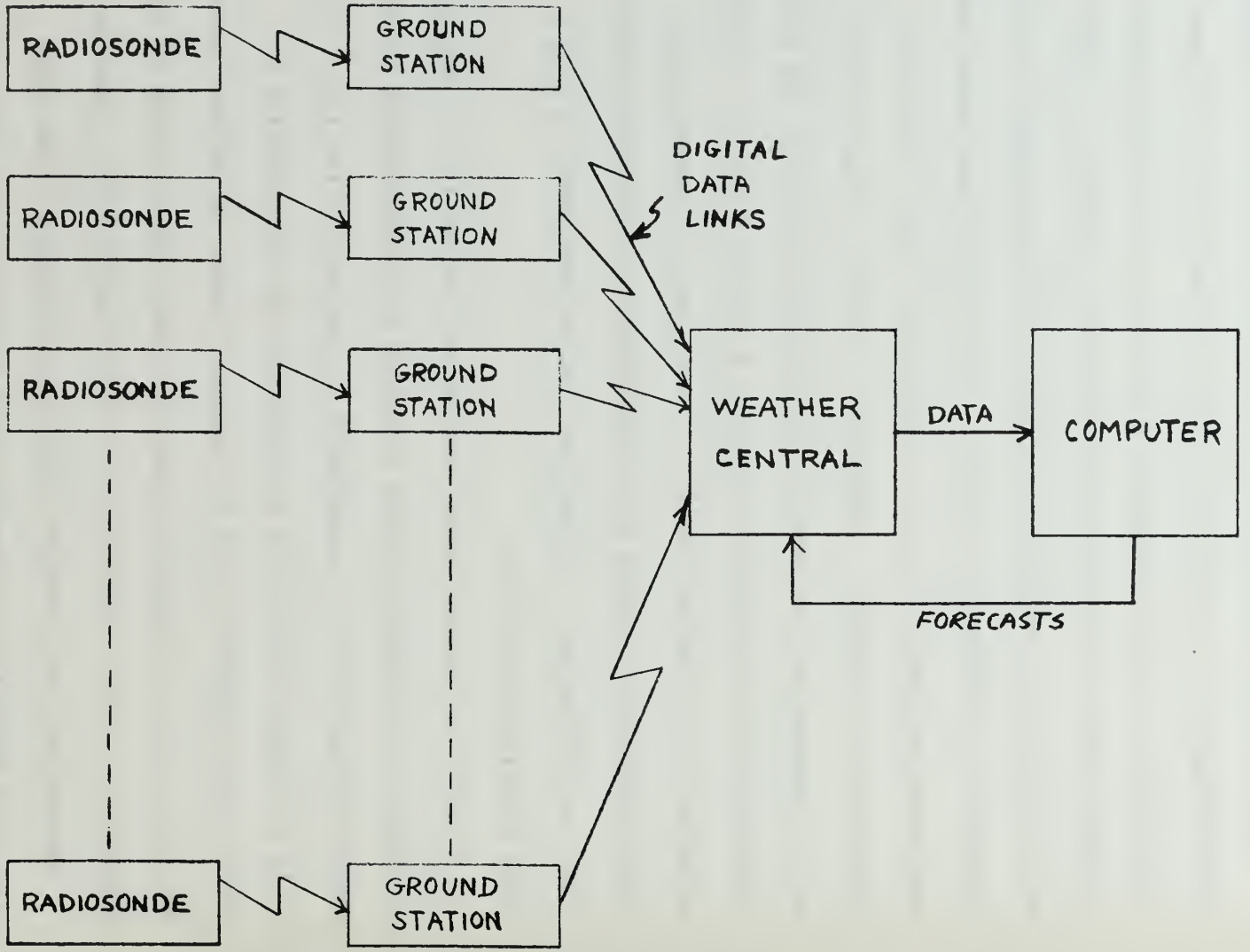


FIGURE 1 RADIO DIGITAL DATA LINK

are to be obtained from radiosonde flights, the entire system must be considered inadequate and improvements must be initiated." This thesis is directed toward accomplishing this overall system improvement.

II. DESIGN CONSIDERATIONS

A complete solid state system will be designed. State of the art techniques and devices will be utilized wherever possible. Table 1 lists the desirable operational specifications of the system.

Power Output	6 watts peak
Modulation	Pulse (PM)
Channel Capacity	Five plus calibrate/sync.
Size and Weight	Minimum
Frequency	403 MHz
Sample Rate	One sample/channel/1.6 sec.
Accuracy	
Temperature	70C to -70C ± .1C
Pressure	1060mb to 5mb ± 1mb
Humidity	10% to 90% ± .1%
Data Format	Digital

TABLE 1

The present radiosonde (AMT-4A), including battery, weighs approximately 2.42 lbs. A minimum weight reduction of 30% is expected while a reduction of over 50% in physical size can easily be achieved. Since the entire system will be solid state a reduction in power requirements is also expected. This could also result in a reduction in battery size and weight. The multiplexer will have a five channel capacity along with a calibration channel which will also be used as a synchronization signal. The calibration information will be used to correct deviations in the received data. These deviations are expected to occur from variations in circuit parameters resulting from the environmental changes over which the radiosonde must operate.

Although meteorological transducers were not considered as part of this investigation, it will be assumed that the temperature and

humidity sensors will be resistance types and the pressure transducer will be a voltage type. These assumptions are based on research presently being done on improved sensors.

Because the radiosonde is expendable, cost must be considered a prime design consideration. Although prototypes are inherently costly, historically, it has been shown that such costs reduce rapidly with usage and improved manufacturing techniques and technology.

III. SYSTEM ENGINEERING CONSIDERATIONS

The following considerations were used in the design of the radiosonde. Fig. 2 shows the overall system block diagram. In this section each circuit will be discussed separately and a detailed analysis given.

A. MULTIPLEXER

A five channel multiplexer will be designed. A sixth channel will be provided for synchronization and calibration. The multiplexer switching cycle is depicted in Fig. 3. Each data channel is sampled every 1.6 seconds for a period of 50 milliseconds. The sync/calibrate channel is 150 milliseconds long. The additional length will enable its detection as the sync pulse. A cycle time of 1.6 seconds is based on the rate of ascent of the balloon and the amount of data required to provide a good profile of the measured meteorological parameters. At this rate data will be obtained approximately every 20 feet.

Since, at the present time, only three parameters are measured, two channels will be unused. However, they are provided in the event other meteorological data is required.

To implement the multiplexer, a relatively new technology in large scale integration will be used. Without this technology the cost, size, and complexity of the multiplexer used in this radiosonde would, in each case, be too great, making it impractical for such a system. Metal Oxide Silicon, an old technology, has made it possible to put a logic system on a single chip [Ref. 11]. The inherent attributes of MOS technology are:

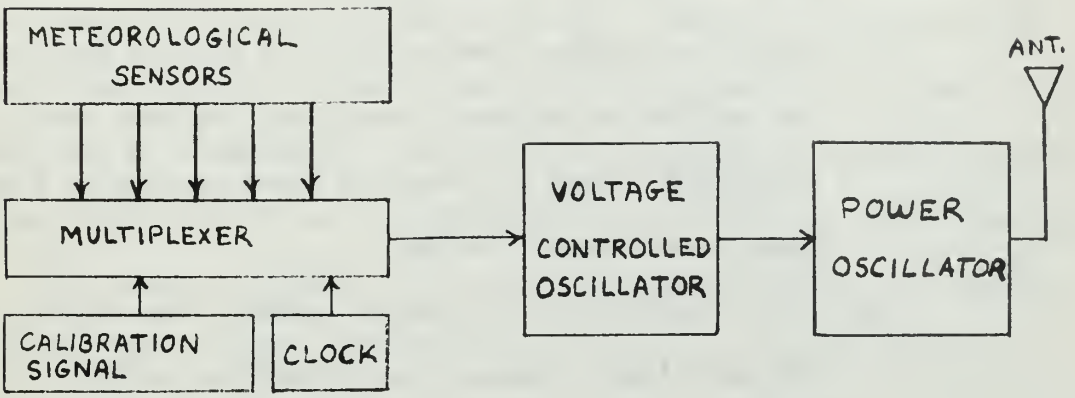


FIGURE 2 SYSTEM BLOCK DIAGRAM

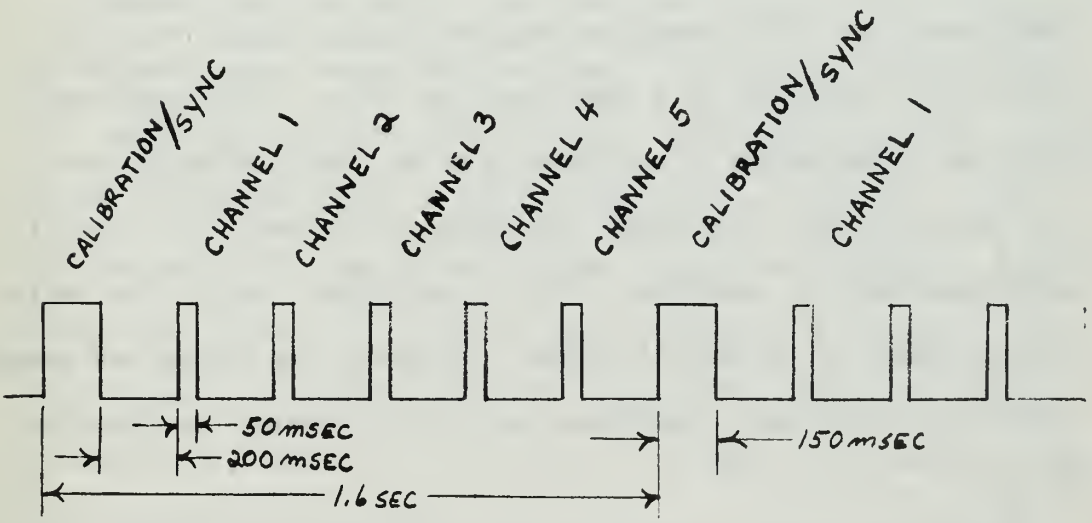


FIGURE 3 MULTIPLEXER SWITCHING CYCLE

a. Small size-device geometry is much smaller than bipolar devices.

b. Low Power Consumption - MOS has the high impedance characteristics of vacuum tubes.

c. Batch Fabrication Processing - this process provides the vehicle to achieve a lower cost per gate function in MOS/LSI arrays and requires fewer processing steps than bipolar manufacturing.

d. Logic Versatility - bilateral current flow in an MOS transistor enhances the versatility of MOS design.

The design or layout of an MOS/LSI system is accomplished by using a family of pre-designed building blocks (cells). The array is customized by arranging the cells in the advantageous positions for interconnection. This procedure ensures optimum usage of silicon surface area resulting in a lower cost per chip. Since engineering costs precluded having a customized chip designed and built during this investigation, a computer simulation of the design of the LSI multiplexer will be performed. This is an actual step in the engineering process of an MOS/LSI system, therefore, the design and computer simulation encompass a significant part of the overall engineering design.

The purpose of the thesis is to design and build a solid state radiosonde. To accomplish this a multiplexer design, differing from the LSI, will be made using discrete MOS IC's. Although bipolar IC's could be used resulting in a significantly fewer number of devices required the author chose to use MOS IC's in order to investigate the operation of such devices over wide temperature and voltage variations.

The clock circuit which will be used to drive the multiplexer will be crystal controlled. The reason for this will become clear in the discussion of the modulation technique. Since a separate and discrete clock oscillator would add cost, weight, and space to the multiplexer the inclusion of the oscillator components on the LSI chip would be most desirable. An effort will be made to design the oscillator with MOS IC's and components which are suitable for integration.

MOS analog switches will be used in the multiplexer to transfer analog data from the meteorological sensors to the modulator. The 'on' and 'off' resistances of these switches should be as low and as high, respectively, as possible in order to minimize data error. Typical 'on' resistances are 250 ohms while values of 60 ohms have been achieved. Typical 'off' resistance values are $1.5 \times 10^{+9}$ ohms.

Summarizing: The analog data from the sensors will be connected to the modulator through MOS switches. The switches will be gated 'on' periodically for 50 milliseconds. Each sensor will be connected to the modulator every 1.6 seconds through the switches. A 200 millisecond 'off' time occurs between successive channels. A calibrate/sync. signal will also be generated each 1.6 seconds. The multiplexer will be designed with discrete MOS IC's to facilitate breadboarding. An MOS/LSI design will be made and a computer simulation performed to ensure proper design. A crystal controlled clock will drive the multiplexer.

B. MODULATION TECHNIQUE

Because of its simplicity to implement, pulse modulation was selected. Other advantages inherent in this technique are lower power consumption and relative noise immunity. Pulse Amplitude Modulation

(PAM), Pulse Code Modulation (PCM), and Pulse Duration Modulation (PDM) were all considered too complex and too costly to implement. It was decided to vary the pulse repetition frequency of the transmitter during the gated 'on' time of each channel. This can easily be accomplished by keying the transmitter with some form of voltage controlled oscillator. This modulation technique will be referred to as Gated Variable Pulse Repetition Frequency.

Using a voltage controlled multivibrator, the pulse frequency of the output will be a function of the input voltages. These voltages are to be derived from each of the meteorological sensors. The oscillator output will key the transmitter. If an oscillator output is required to turn the transmitter on then, if no oscillations occur during the time the sensors are not being sampled, the transmitter will be off, resulting in a considerable savings in power. Fig. 4 presents an overall picture of the relationship between sampled voltages generated from the sensor circuits and the output of the voltage controlled multivibrator. Note that the voltage sampled for the calibrate signal is constant. The number of pulses generated during the 50 millisecond 'on' time can be counted, after detection, in the receiver. This count can be converted directly to frequency and if the frequency/voltage characteristics of the VCM are known the data can be converted directly to their respective meteorological parameters. The reason for the crystal controlled clock in the multiplexer now becomes clear. Since the 'on' gate to the VCM will be set at 50 milliseconds, the number of pulses counted during this time is a direct frequency measurement. Once the count has been performed, it

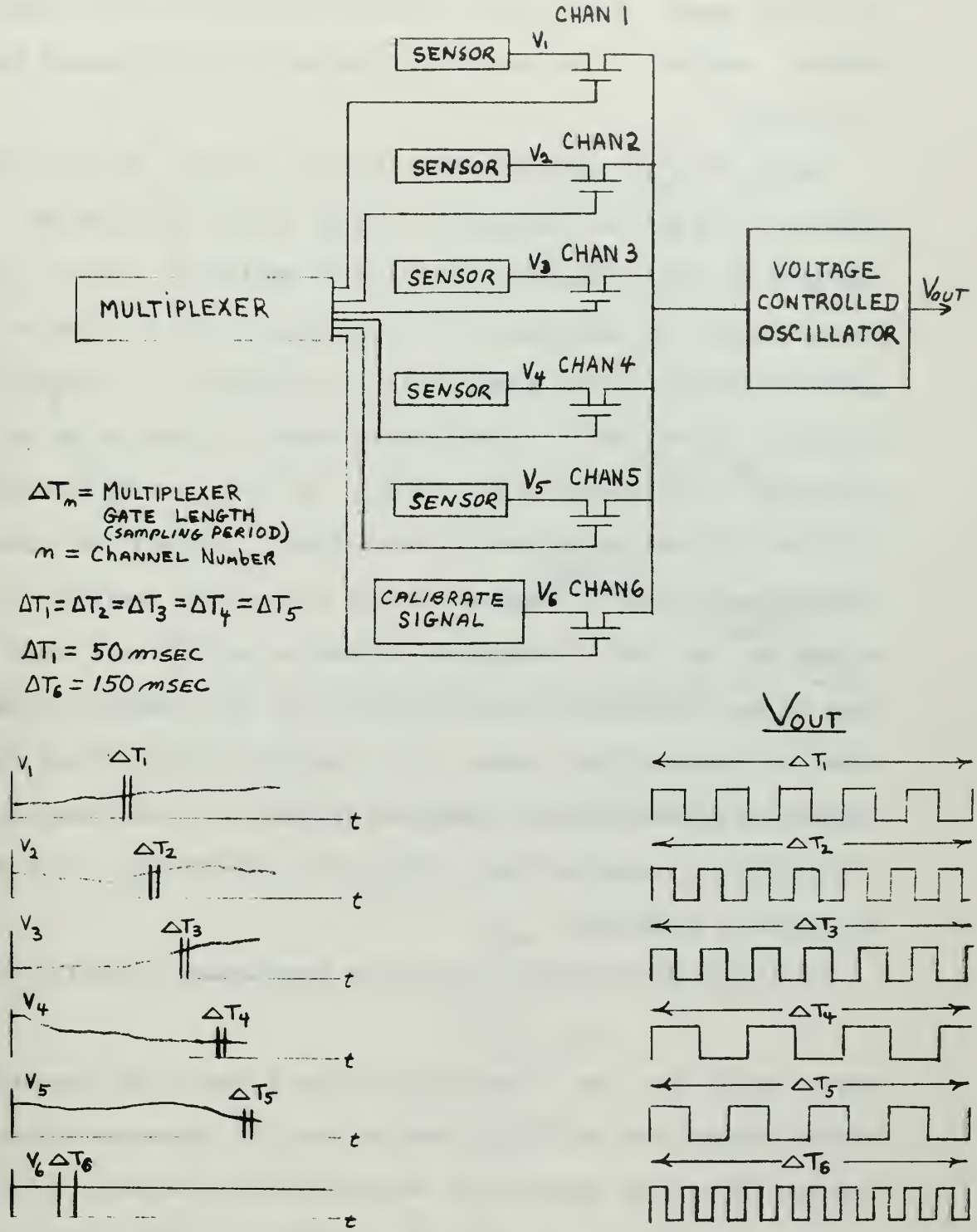


FIGURE 4 MULTIPLEXER AND VCM BLOCK DIAGRAM

can be stored on magnetic tape or punch tape in digital form. There is no requirement for any analog to digital conversion at the ground station. Decoding of the data in the receiver will be discussed further in Section IX.

Ideally, the VCM characteristics should be linear. Any non-linear characteristics must be predictable in order to have the computer interpret the data correctly. Linearity is realizable, however, since the radiosonde will be subjected to a wide temperature environment, a definite drift in the VCM characteristics is expected. In order to compensate for this drift, a calibration channel is provided by the multiplexer. This channel has a 150 msec 'on' gate, and it is during this time that the VCM drift will be monitored. This will be accomplished by measuring the frequency change with a known constant voltage into the VCM. The constant voltage source will be a zener diode or some similar device which will put the VCM somewhere in the center of its operational range. Fig. 5 depicts the anticipated VCM-temperature characteristics. Note that by monitoring the frequency out of the VCM with a constant input voltage, the new characteristics can be completely determined.

The linear VCM characteristics can be represented by the function:

$$y = ax + b$$

where a equals the slope in Hz/volt and where b equals the theoretical offset frequency for zero volts input to the VCM. Since the voltage into the VCM will be derived from the meteorological sensors, then the conversion from frequency to the value of the measured parameter will be relatively simple. The information contained in the calibration

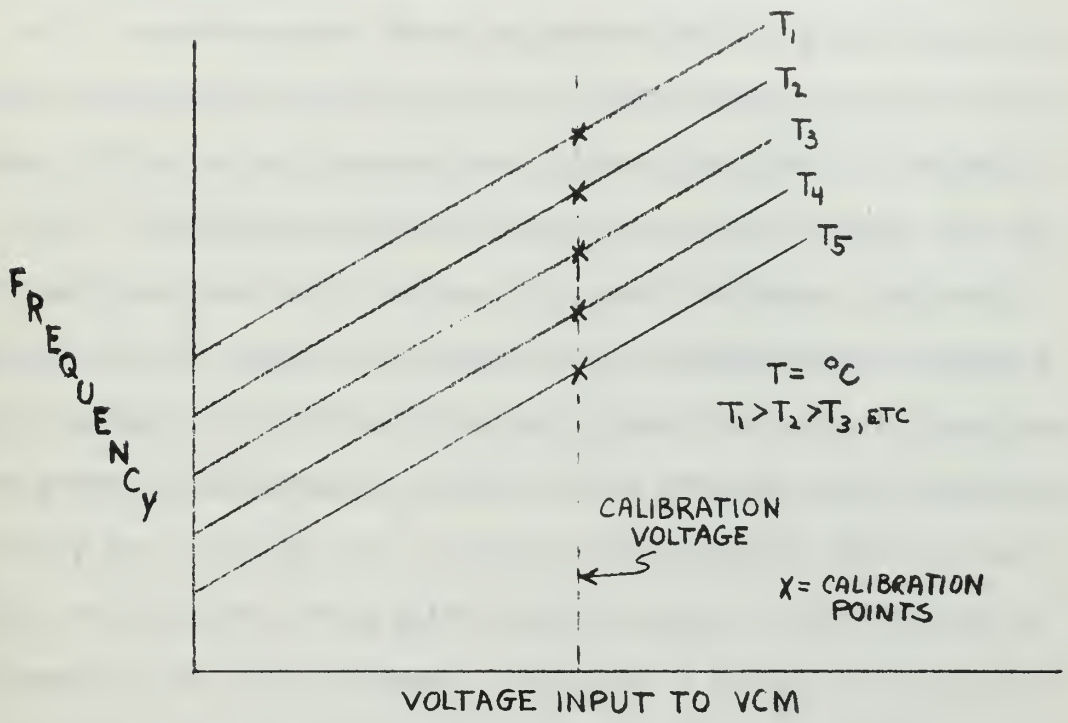


FIGURE 5 IDEAL VCM CHARACTERISTICS

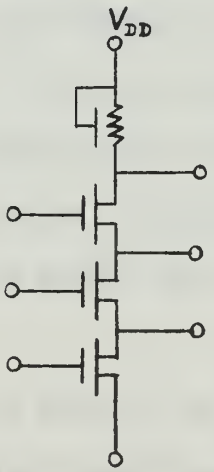


FIGURE 6 3102- THREE INPUT GATE (MOS IC)

pulse will allow the computer to update the offset, b, during each data cycle. Ideally, the slope a will not change throughout the operational flight.

In summary: the analog data from the sensors will be connected to Voltage Controlled Multivibrator by MOS analog switches. Since the 'on' gates of each channel and the calibration/synchronization pulse are of fixed time periods, the frequency out of the VCM during the 'on' time is determined simply by counting the pulses. This information, in digital form, can be either stored or fed directly to a computer for calculation of meterorological data. The 150 millisecond calibration pulse will monitor any drift in the VCM frequency-voltage characteristics and will also be used to identify the beginning of a data cycle for synchronization purposes. The design of the VCM will be completely solid state with cost being prime consideration. This will limit the number of electronic components used and also require some consideration as to the cost of each of the components.

C. TRANSMITTER

Regardless of the fact that the present cost of high power, high frequency transistors is prohibitive, it was decided to build a solid state transmitter. The reason for this is the anticipation of lower cost devices in the near future resulting from improved technology and manufacturing techniques. In addition, a single stage, transistor power oscillator will help reduce overall system weight, size, and power consumption.

The transmitter is to be keyed on and off by the VCM. To ensure positive keying, the power supply will be removed and reconnected

to the transmitter through a transistor switch. One or more additional switching transistors may be required to accomplish this.

D. POWER REQUIREMENTS

Little consideration could be given to overall power requirements prior to breadboarding the system. However the voltage requirements of MOS/LSI integrated circuits are approximately -27 volts and -13 volts. It was decided to use the -27 volts as the primary power for the entire system. A 27 volt battery with a 13.5 volt tap can be utilized as a power source. The present battery provides 114 volts, 7.0 volts, and 3.0 volts. It may be possible to realize a reduction in battery size and weight resulting from a reduced power requirement.

IV. DETAILED SYSTEM DESIGN

The following sections give a detailed description of the design of each part of the system.

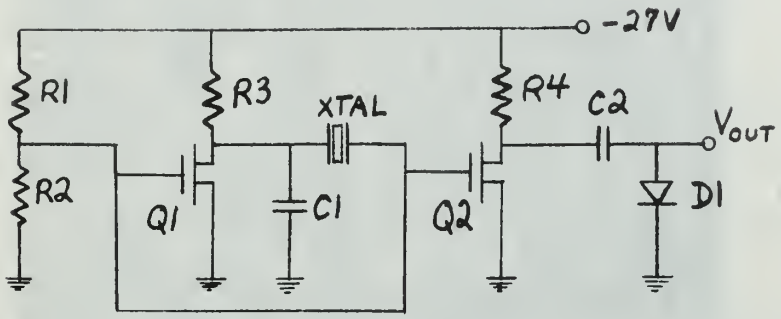
A. THE MULTIPLEXER

Two circuit designs were made. One was from presently available MOS IC's to facilitate breadboarding. The other design was accomplished using computer-aided design, a basic step in the process of building an MOS/LSI chip. All the steps up to customizing the layout of the chip were performed. Each of these designs will be discussed below.

1. Crystal Oscillator

The circuits common to both multiplexer are the crystal oscillator and frequency divider. As mentioned previously, it would be desirable to include the oscillator on the multiplexer chip. A MOS IC type 3102, was used as the basic building block in the design of the oscillator. The 3102 is a 3 input gate and its schematic is shown in Fig. 6. Each gate is a MOS transistor capable of amplification. The oscillator circuit which was designed is shown in Fig. 7.

R1 and R2 form a voltage divider to bias Q1 and Q2. Q1 is the oscillator while Q2 acts as a buffer. C2 is a 30 picofarad coupling capacitor while C1 provides for the proper phase of the signal fed back to the gate of Q1 to cause oscillation. D1 serves to clamp the output signal at zero volts. This is necessary to insure switching of the MOS flip-flop which will be driven by the oscillator. Fig. 8 shows the actual output of the oscillator/buffer.



R1 = 240K Ω
R2 = 68K Ω
R3 = 22K Ω
R4 = 12K Ω

C1 = 75 PF
C2 = 30PF

FIGURE 7 CRYSTAL OSCILLATOR AND BUFFER SCHEMATIC

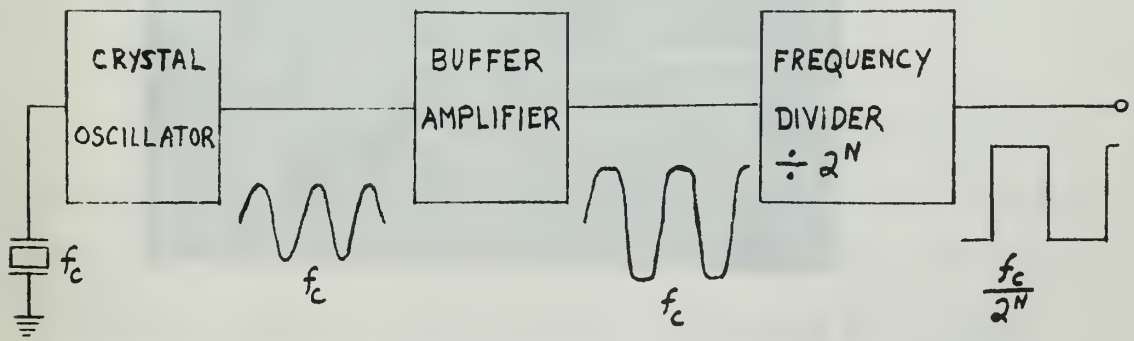


FIGURE 9 CRYSTAL OSCILLATOR AND FREQUENCY DIVIDER BLOCK

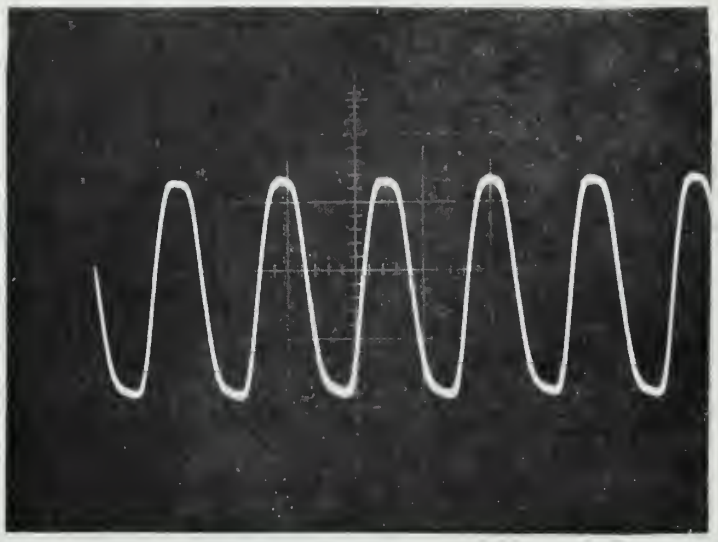


FIGURE 8 CRYSTAL OSCILLATOR AND BUFFER OUTPUT WAVEFORM

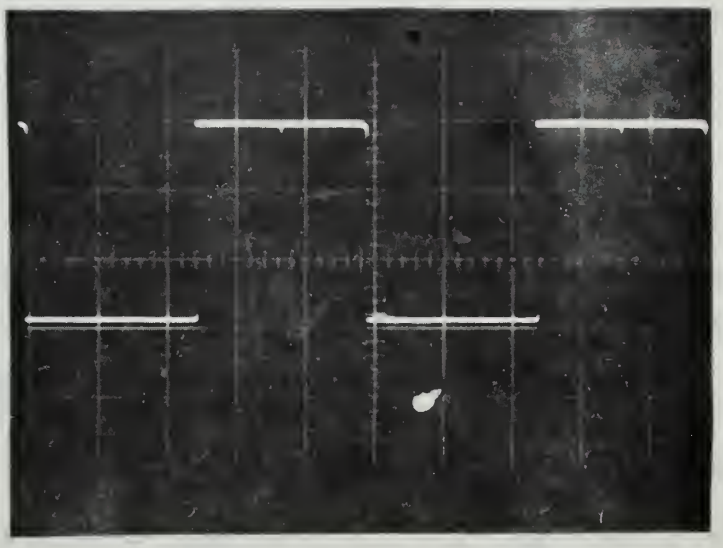


FIGURE 10 FREQUENCY DIVIDER OUTPUT WAVEFORM

The nonlinearity in the waveform is of no consequence since it will only be used for switching. The frequency of oscillation in this case was 324.4 KHz and the amplitude was minus 16 volts. It should be mentioned that the crystal in the oscillator circuit is operating in its shunt resonant mode.

Integration of the oscillator/buffer onto the multiplexer chip is possible. Each component is capable of being integrated on a silicon chip with the exception of the crystal and C1.

2. Frequency Divider

A simple frequency divider was built using flip-flops in series operating in a toggle mode. For fourteen stages (2^{14} = 16384) the frequency was divided down to approximately 19.8 Hz which was sufficiently close to the desired value of 20 Hz for simulation purposes. The final single chip design is intended to have an oscillator frequency of 655.36 KHz with a fifteen stage frequency divider. This was decided after considering the werrent frequency characteristics of MOS devices. Fig. 9 depicts the oscillator and frequency divider and Fig. 10 is an actual photograph of the clock signal at the output of the final divider stage.

3. Breadboard Multiplexer

Fig. 11(a) is a block diagram and Fig. 11(b) is the printed circuit board IC layout of the actual multiplexer built in the laboratory. All devices used were Fairchild MOS IC's. The shift registors are IC# 3101 (Dual JK Flip-Flop) and all the gates are IC# 3100 (Dual Five Input Gate). The operation of the circuit is as follows:

The clock pulse (generated from crystal oscillator and frequency divide as shown in Fig. 9) passes through G2

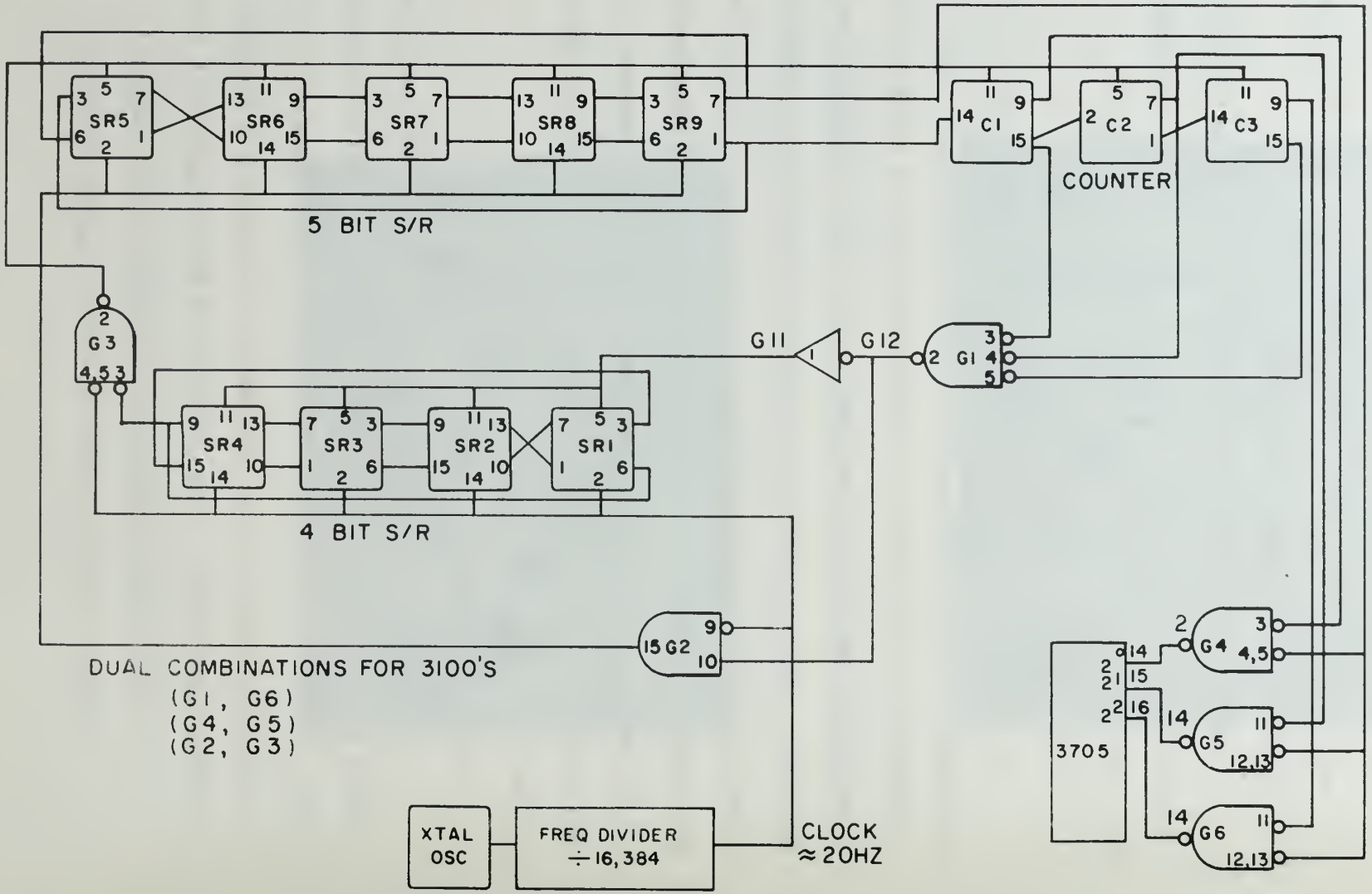


FIGURE 11a DISCRETE MULTIPLEXER BLOCK DIVIDER

TOP VIEW

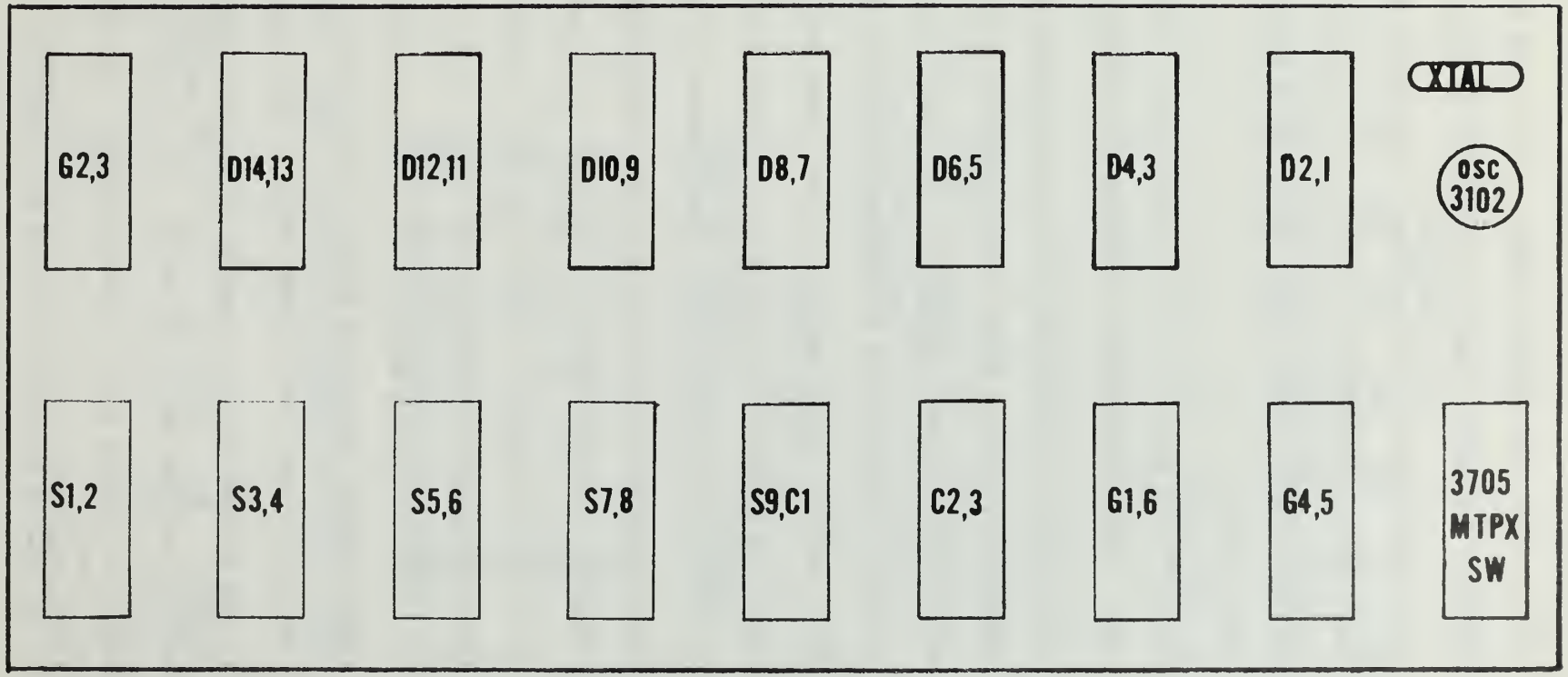
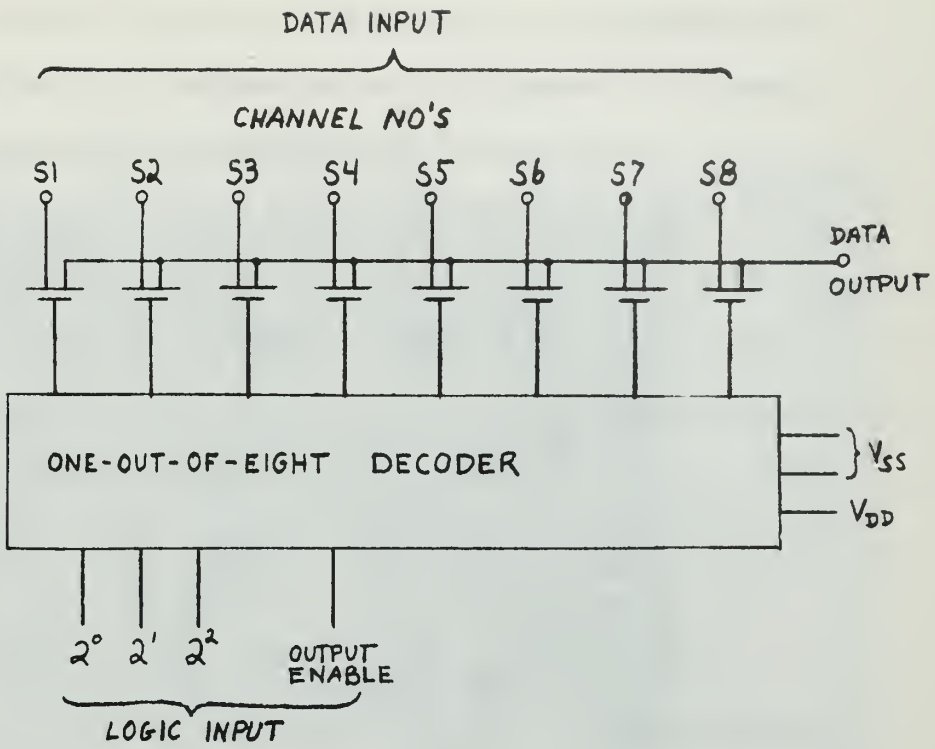


FIGURE 11b DISCRETE MULTIPLEXER LAYOUT

and steps the five bit shift register (S/R), SR5 through SR9, so that the output of SR9 (pin 1) goes high (OV) every 200 milliseconds. Counter C1 through C3 changes state each time SR9, pin 1, goes high. The output states of the counters are transmitted through G4, G5, and G6 to an 8-channel MOS multiplex switch (3705) only while pin 7 of SR9 is low.

When SR9 pin goes high, the three inputs to the 3705 go high. Fig. 12 shows the diagram and truth table for the 3705. S8 is grounded so that during the 200 milliseconds between the channel gates zero potential appears at the data output channel. Since pin 7 of SR9 is low for only 50 milliseconds, each state of the counters appear at the inputs for this length of time. When the counters reach the state HLH the output of G1 goes low causing G2 to inhibit the clock pulse. Simultaneously, the clear direct inputs to the 4 bit S/R, SR1 through SR4, go high allowing the clock pulse to step the low state in SR1 to SR4 in 115 milliseconds. Pin 7 is held low during these 150 milliseconds allowing S6 to remain 'on'. When pin 9 of SR4 goes low a clear direct input is generated synchronously through G3 putting the counter and SR5 through SR9 back into a high state. The clock pulse is now allowed to pass through G2 stepping the five bit S/R and is also inhibited by G3. The inverted output (G11) is now low which clears the four bit S/R until the counter again recycles to the HLH state.



TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S1
H	L	L	H	S2
L	H	L	H	S3
H	H	L	H	S4
L	L	H	H	S5
H	L	H	H	S6
L	H	H	H	S7
H	H	H	H	S8
X	X	X	L	OFF

FIGURE 12 3705 - (MOS IC) DIAGRAM AND TRUTH TABLE

FIGURE 13 DISCRETE MULTIPLEX CYCLE

From the above it is seen that S6 becomes the 150 millisecond calibration/sync. gate while S8 is the 200 millisecond 'off' gate. Channels one through five are represented by S1 through S5 respectively. Fig. 13 depicts the generated multiplex cycle. The photograph shown in Fig. 14 was taken at the data output terminal of the 3705 device. All data input terminals were connected to a common source voltage of six volts. The sweep speed is 200 milliseconds per centimeter and the vertical sensitivity is two volts per centimeter. The photograph clearly shows that the multiplexer operates as anticipated.

4. LSI Multiplexer

The primary reasons for designing the LSI chip is to learn the approximate size and complexity, in addition to realizing an actual design. Size and complexity, in general, determine the cost of the chip. Of course, the market usage is also a primary factor, however, in the case of the radiosonde, there is no doubt that these requirements will equal or exceed any LSI device utilized on the market to date. If this chip design were not included as part of this thesis, final estimates of system cost, size, weight, and other factors considered important would not be realistic.

Utilizing Computer Aided Design (CAD) to perform logic simulation, a multiplexer was designed using predesigned and pre-characterized cells. These cells are available in the computer and are called by using a pre-specified format. The computer simply connects all the cells as directed in the program. After the network has been completely described an input test sequence can be applied to the system. Outputs can be monitored at any point

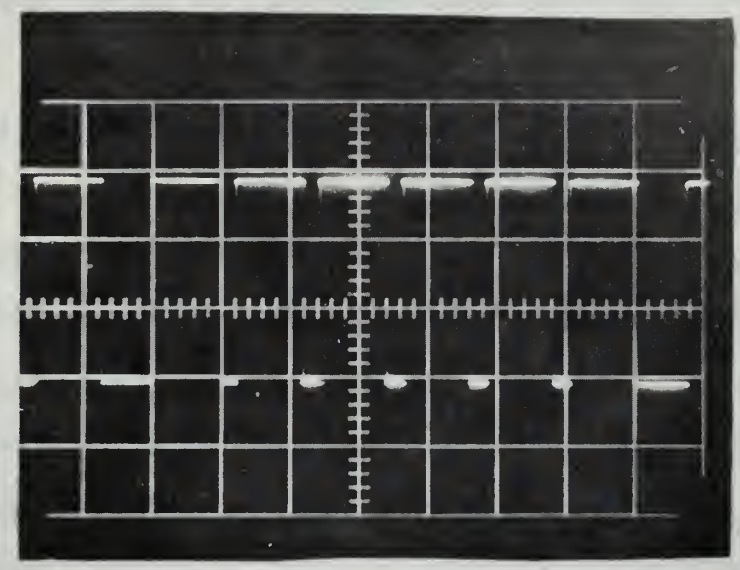
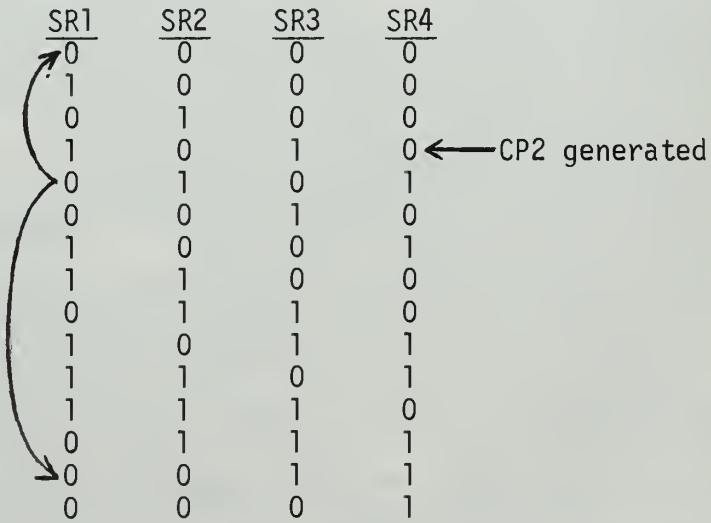


FIGURE 14 EXPERIMENTAL OUTPUT OF DISCRETE MULTIPLEXER

in the network to ensure proper operation. The final phase of the CAD is a circuit topology layout and artwork generation. This phase of the design was not accomplished since the information sought by performing the LSI design could be determined without it.

Fig. 15 is the logic diagram of the network which was simulated on the computer. This network was designed using the cells from the standard circuit library. The network operation is as follows:

> SR1 through SR4 make up a modulus 15 counter with a parallel entry capability. They are driven by a clock generator whose input is the 20 Hz signal from the frequency divider previously discussed. The clock generator provides two clock signals, 180° out of phase, to drive the masterslave flip-flops SR1 through SR4. All blocks prefixed by SR are master-slave flip-flops. The MOD 15 counter generates the following sequence:



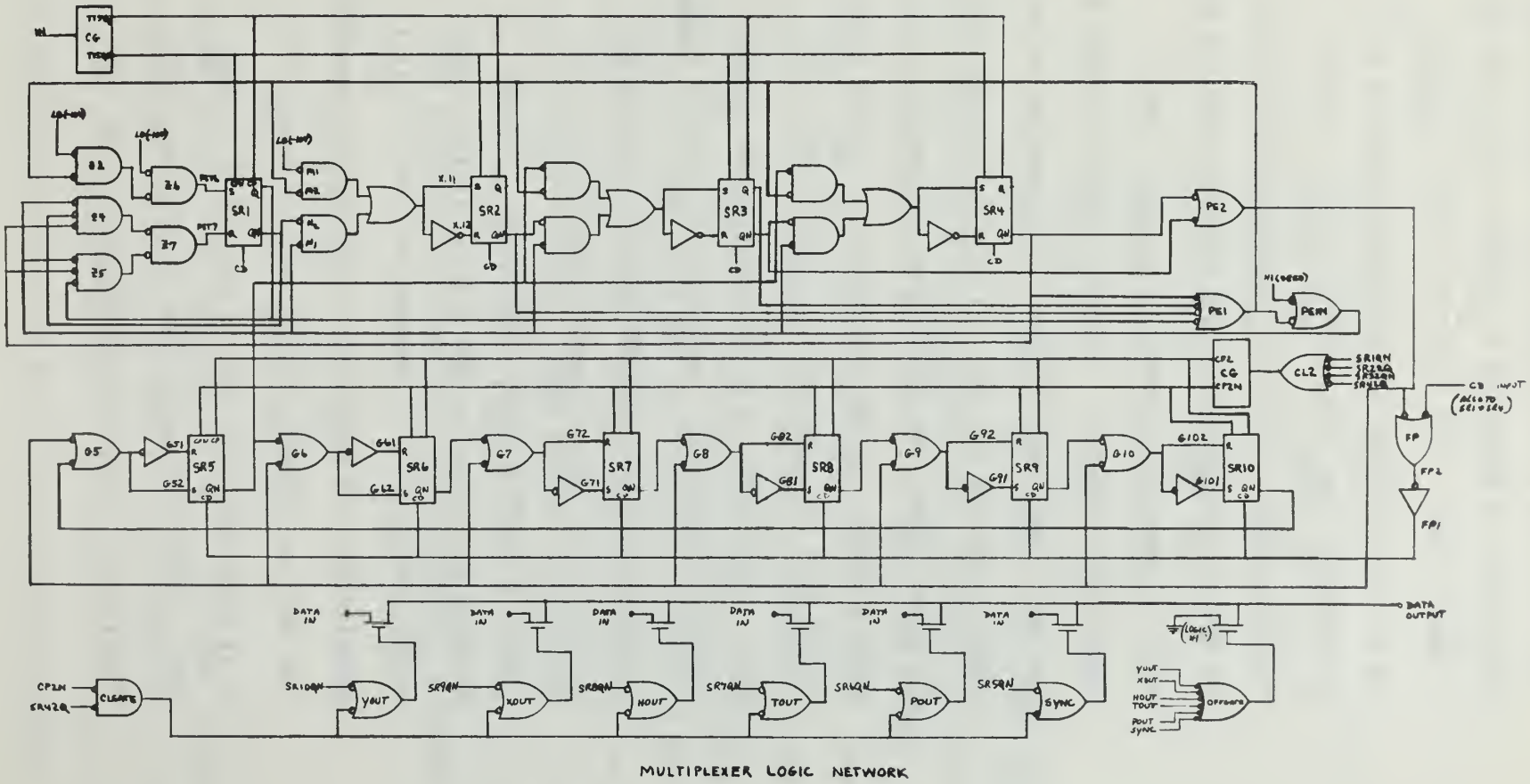


FIGURE 15 LOGIC DIAGRAM OF LSI MULTIPLEXER

SR5 through SR10 is a six bit shift register whose clock pulse is generated by decoding the state 1010 as shown above. Each time this state is decoded the six bit S/R, one stage of which contains a '1' (all others being '0'), shifts the '1' to the following stage. The next incoming clock pulse to the MOD 15 counter shifts the state to 0101 and this state is decoded to provide a 'parallel enable' input to the counter. The next clock pulse puts the counter in the state 0000 or 0011 depending on the state of the six bit S/R. If the six bit S/R is in any state other than 100000 then the counter will shift to 0000. If the six bit S/R is in the state 100000 then the counter will shift to the state 0011. These shifts are indicated on the counter sequence shown above. Note that the counter changes state every 50 milliseconds and that for the six bit S/R in any state except 100000 SR4 goes low (logic '1') every fifth clock pulse. Then by decoding the output of SR4 and the states 010000, 001000,000100, etc., a sequence of five 50 millisecond gates are generated. Each gate is separated from the one following by 200 milliseconds. Also it is seen that when the six bit S/R is in the state 100000 the counter goes to the state 0011 resulting in the output of SR4 staying low for

two additional clock periods for a total of 150 milliseconds. The logic equations for the multiplex cycle are:

$$\text{Calibrate/sync.} = SR5 \cdot SR4$$

$$\text{Channel one} = SR6 \cdot SR4$$

$$\text{Channel two} = SR7 \cdot SR4$$

$$\text{Channel three} = SR8 \cdot SR4$$

$$\text{Channel four} = SR9 \cdot SR4$$

$$\text{Channel five} = SR10 \cdot SR4$$

$$\text{Offgate} = \overline{SR5} \cdot \overline{SR6} \cdot \overline{SR7} \cdot \overline{SR8} \cdot \overline{SR9} \cdot \overline{SR10}$$

The purpose of the offgate is to ensure that the analog output lead is at zero potential during the time all of the other channels are off. The logic high notation at the input of the offgate switch in Fig. 15 indicates the permanent zero potential connected at that point. The logic equations above are depicted at the bottom of the figure by the seven NOR gates and just above the gates are their respective MOS analog switches. In the computor simulation network time delays are also included. After several simulations, it was learned that these delays caused slight variations in the 'on' gate lengths. This difficulty was overcome by generating a clockgate (CLGATE) where

$$CLGATE = SR4 \cdot CP2 \quad \text{and}$$

$$CP2 = SR1 \cdot \overline{SR2} \cdot SR3 \cdot \overline{SR4}$$

This is shown in the lower left hand corner of the logic diagram. Another feature of the design is the fact that, regardless of the initial states of the counter and S/R, the counter will only complete one cycle before the system will fall into its proper operating

frequency. This is accomplished by decoding a parallel enable signal (PE2) to set the six bit S/R into the 100000 state. Logically, as shown in the diagram

$$PE2 = SR3 \cdot SR4$$

on the center right side of the diagram we have an external CD signal input which was only used to satisfy the computer requirements that all states must be initialized to some logic level. In an actual system this will not be required.

Not included in Fig. 15 is the network shown in Fig. 16 which depicts the crystal oscillator and frequency divider circuits which are actually part of the multiplexer. Note that the output of the frequency divider feeds the stage that is shown in the upper left corner of Fig. 15.

Appendix A shows the CAD source program and simulation program for the multiplexer. Appendix B shows the computer printout every 30 time-units which represents an input clock period. From the printout it is seen that the correct sequence of gates is continuously generated after the first cycle of the multiplexer. A logic '1' indicates that the output of the respective gate is at the state which closes the analog switch. For example, a '1' appearing in the POUT column means that the output of the gate labeled POUT in Fig. 15 is at the voltage level required to close the gate to which it is connected. Any analog data appearing at the input of this gate will appear at the data output lead. Since all other gate outputs are '0', all other switches will be open. Note that the 'off gate' switch is closed during the time that all other gates are open.

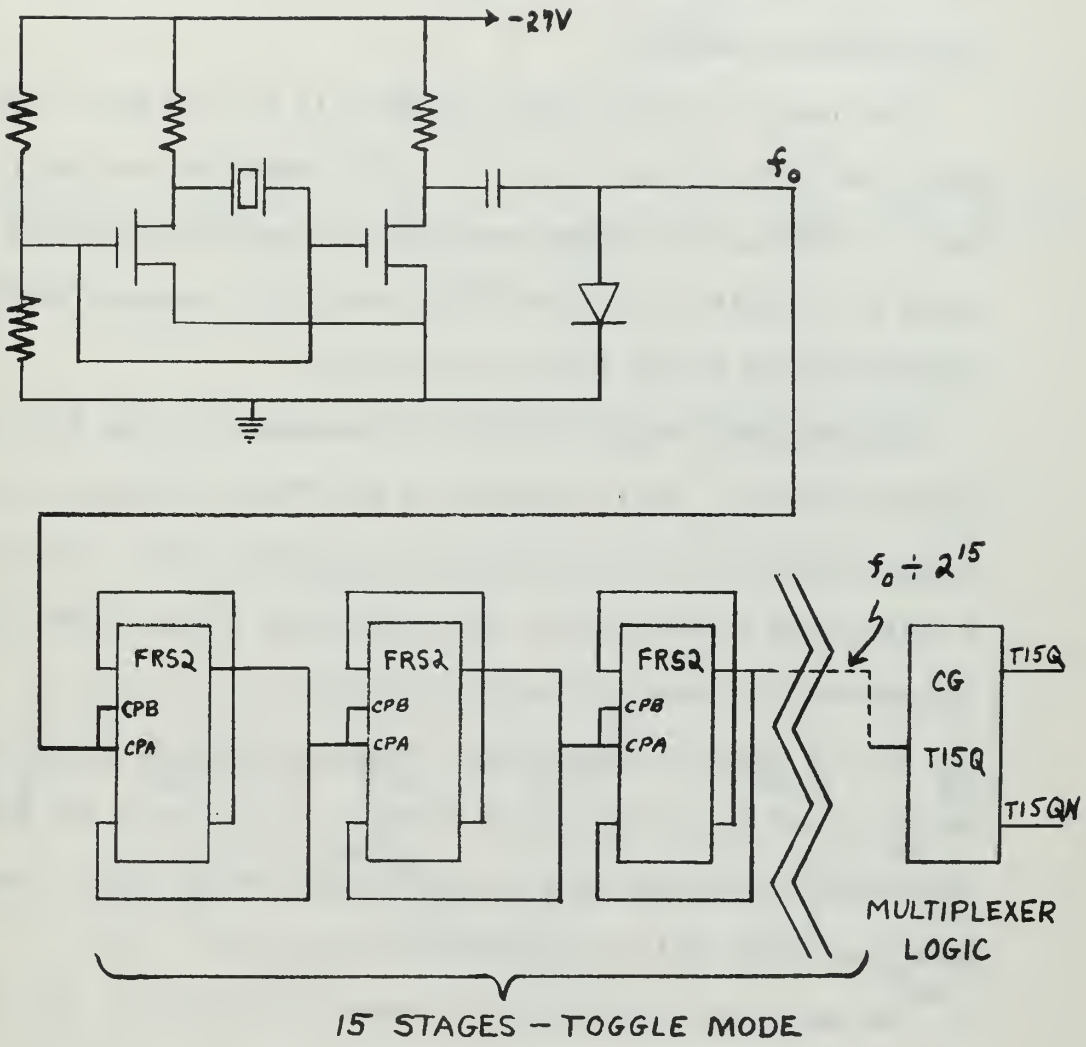


FIGURE 16 CRYSTAL OSCILLATOR AND FREQUENCY DIVIDER SCHEMATIC

B. MODULATOR

The modulator consists of a Voltage Controlled Multivibrator (VCM) and two switching transistors. The transmitter (Power Oscillator) is turned on and off at the VCM frequency. The VCM frequency is dependent upon the input voltage which is a function of the meteorological sensors.

The range of the VCM input voltage will be from minus five to minus ten volts (-5 to -10 volts). This range was selected on the basis of the maximum recommended input voltage for MOS analog switches which is -10 volts. Over the above range, the frequency/voltage characteristics of the VCM will be linear.

The frequency range of the VCM is determined by the Receiver characteristics. The IF bandpass in the SMQ-1A, Radiosonde Receiver is approximately 900 KHz. Using this knowledge and a requirement for a fairly good reproduction of the transmitted pulses in the receiver the maximum VCM frequency was set at 80 KHz.

Fig. 17 shows the theoretical frequency spectrum of the transmitted signal at a frequency of 80 KHz. The S/N ratio and the reproduction should be good over this range of operating frequencies. Data resolution will be discussed in section VI.

The basic VCM configuration is shown in Fig. 18(a). Q3 and Q4 provided constant current to charge C1 and C2. R2, R3, C1, and C2 determine the frequency of oscillation. D1 and D2 are included to prevent emitter to base reverse voltage breakdown due to the abrupt 27 volt change in the collectors of Q1 and Q2.

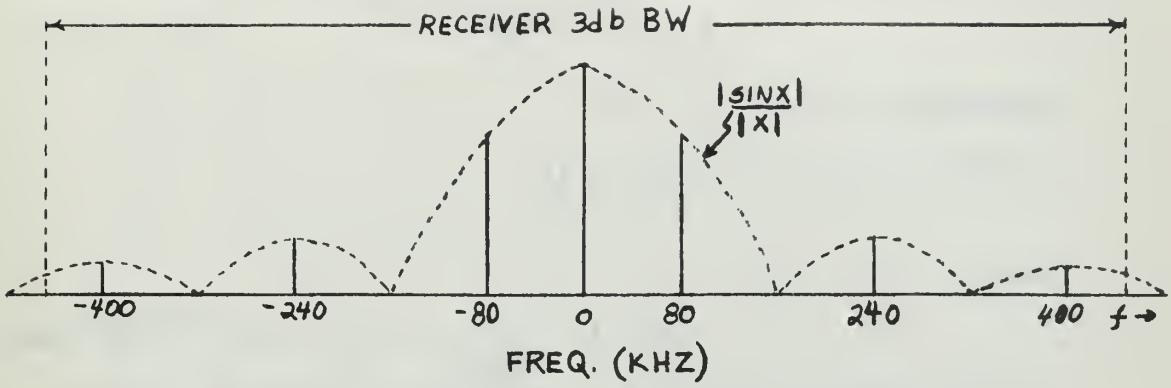


FIGURE 17 TRANSMITTER FREQUENCY SPECTRUM

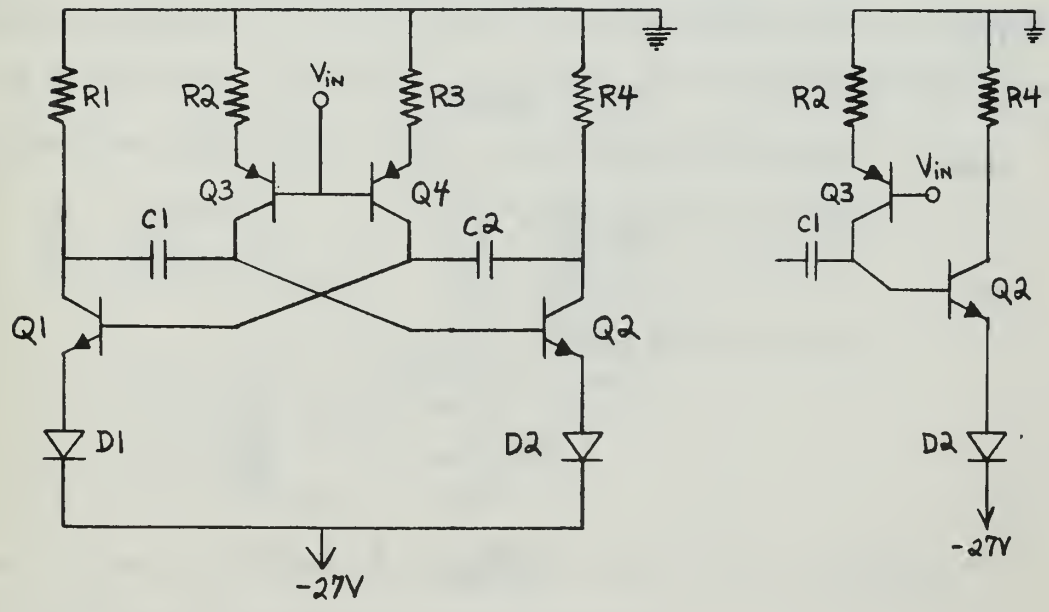


FIGURE 18 VCM SCHEMATIC

The values of the circuit elements are determined in the following manner. In Fig. 18(b) assume V_{in} = -10 volts and ΔV across C1 = 27 volts and V_{be} (on) = .7 volts. Then:

$$I = \frac{0-(-10+.7) \text{ volts}}{R2}$$

and also

$$I = C1 \frac{\Delta V}{\Delta t}$$

where

$$\Delta t = \frac{1}{2} \cdot \frac{1}{80KHz} = \frac{12.5}{2} \text{ usec} = 6.25 \text{ usec}$$

the half cycle time of the upper frequency .

$$\therefore \quad I = C1 \frac{\Delta V}{\Delta t} = \frac{9.3}{R2}$$

or

$$R2C1 = \frac{9.3\ [6.25]}{27} \text{ usec}$$

$$= 2.15 \text{ usec}$$

let

$$C1 = 100 \text{ pf}$$

then

$$R2 = 21.5 \text{ K}\Omega$$

For

$$V_{in} = -5 \text{ volts}$$

$$I = \frac{0-(-5+.7)}{R2} = C1 \cdot \frac{27}{T/2}$$

$$\therefore \quad T = \frac{54\ R2\ C1}{4.3} = 27 \text{ usec}$$

The lower frequency output of the VCM is:

$$f = \frac{1}{27} \text{ usec} = 37 \text{ KHz}$$

The circuit was breadboarded and the final design values are (referring to Fig. 18[a])

R1 = R4 = 5.1 K Q3 = Q4 (Fairchild 2N4250)

R2 = R3 = 22 K Q1 = Q2 (Fairchild 2N3643)

C1 = C2 = 120 pf

C. TRANSMITTER

A solid state power oscillator in a modified Colpitts (Clapp) configuration was built using a Fairchild Type MSA8046 power transistor.

Fig. 19(a) shows the actual circuit configuration and parameter values.

Fig. 19(b) is the AC equivalent circuit. The primary frequency determining elements are C1 and L1. C4 controls the amount of regenerative feedback. C2 series tunes the output tank which is connected to a 50 ohm load. Cbc, Cbe, and Cce are all the interal capacitances of the power transistor. The circuit element values are:

R1 = 1.3KΩ1W
R2 = 200Ω .5W
R3 = 5Ω5W(wire wound)

C1 = .4pf to 4 pf variable
C2 = .9pf to 7 pf variable
C3 = 430 pf
C4 = 8pf
C5 = 1000pf (feed through)

L1 = 2 1/2 turns #16 wire
3/8" diam., 3/16" spacing
L2 = 1 turn #16 wire
1/2" diam.
L3 = 6.7 micro henry RF choke

The RF choke (L4) shown in Fig. 19(a) is due to the inductance of the 5 ohm wire wound resistor listed above.

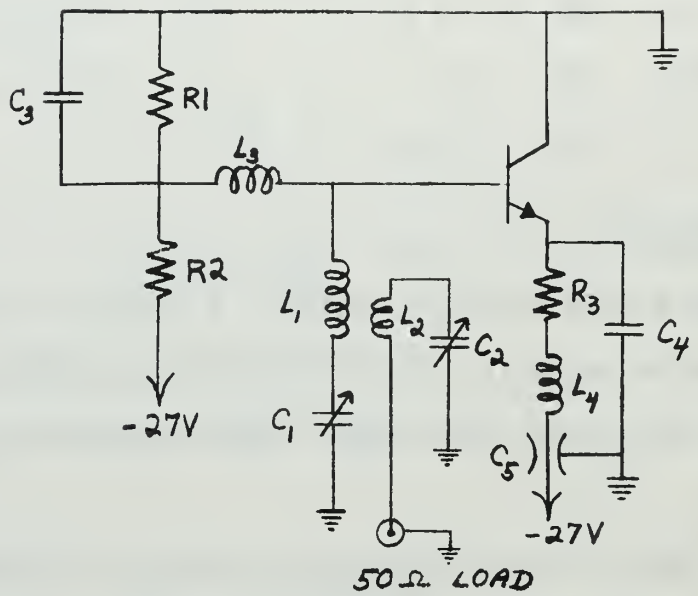


FIGURE 19a POWER OSCILLATOR SCHEMATIC

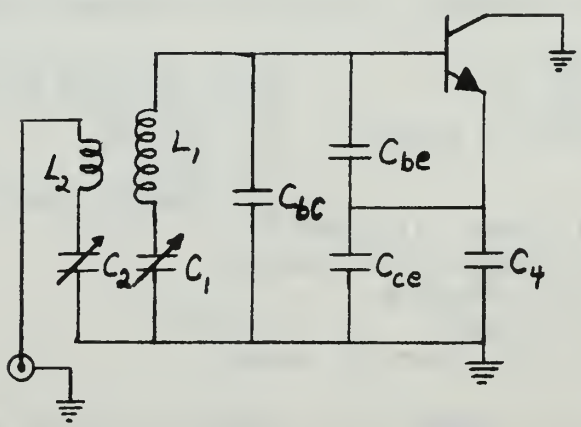


FIGURE 19b POWER OSCILLATOR RF EQUIVALENT CIRCUIT

The CW power output of the oscillator is six watts. Current drain is approximately 750 milliamperes for an efficiency of:

$$100 \times \frac{6}{.75 \times 27} = 29.6\%$$

The current drain is rather arbitrary from device to device. Another power oscillator was built and a power (CW) output of seven watts was obtained with a current requirement of only 600 milliamperes.

For positive switching of the power oscillator a Fairchild 2N2657 switching transistor was inserted in the emitter circuit. In order to provide the drive for the 2N2657, a 2N3643 transistor was put between the switch and the VCM. Fig. 20 is an overall schematic diagram of the radiosonde modulater and transmitter section. The transistor layout for the modulator and transmitter chassis is shown in Fig. 21. Fig. 22 and Fig. 23 show the actual oscilloscope presentations of the 400 Megahertz carrier envelope (top sweep) and the switching waveform at the collector of the 2N2657 (bottom sweep). Fig. 22 was taken at the low end of the VCM range (approx. -6 volts input), and Fig. 23 was taken at the upper end (approx. -10 volts input).

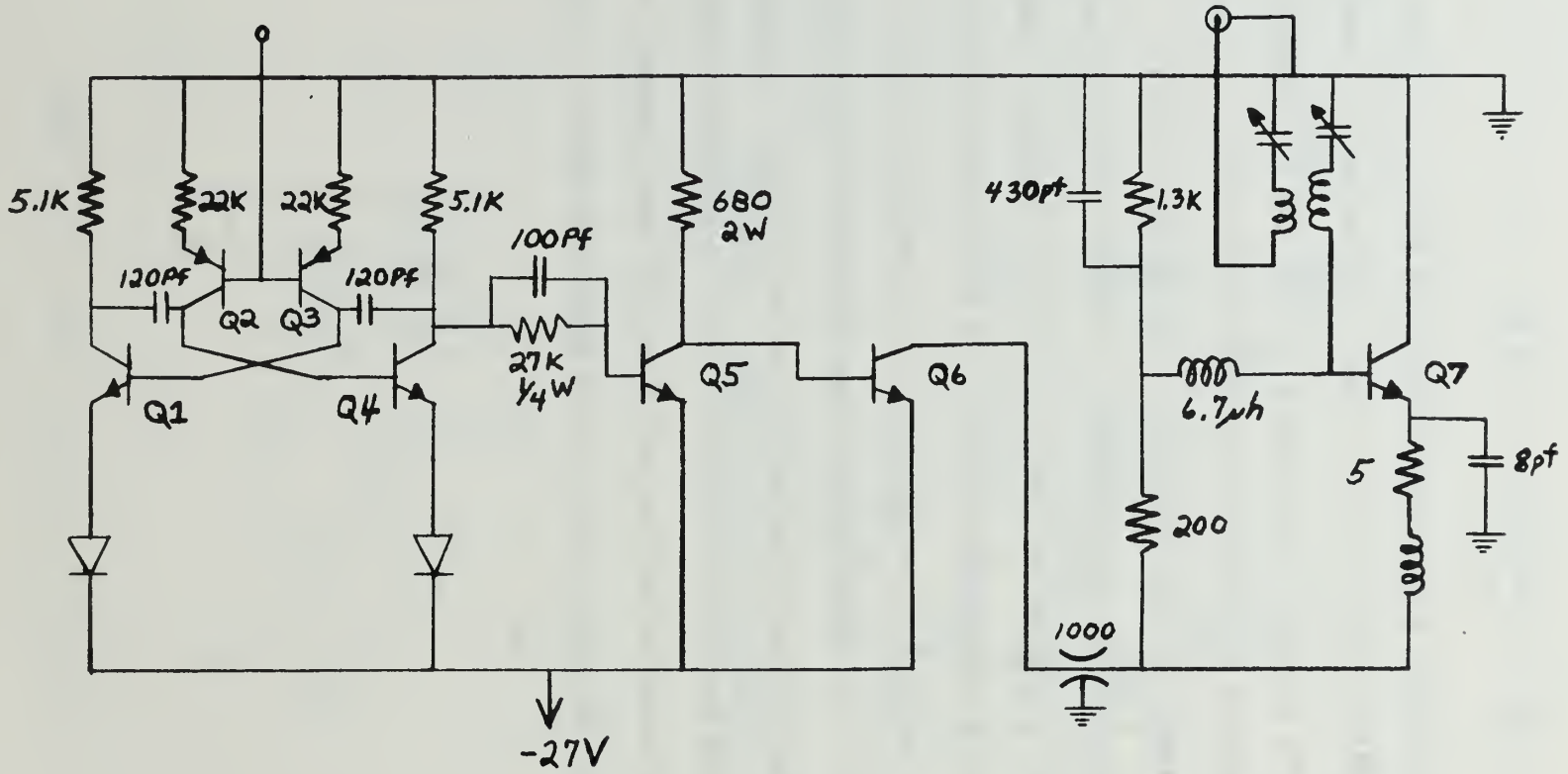
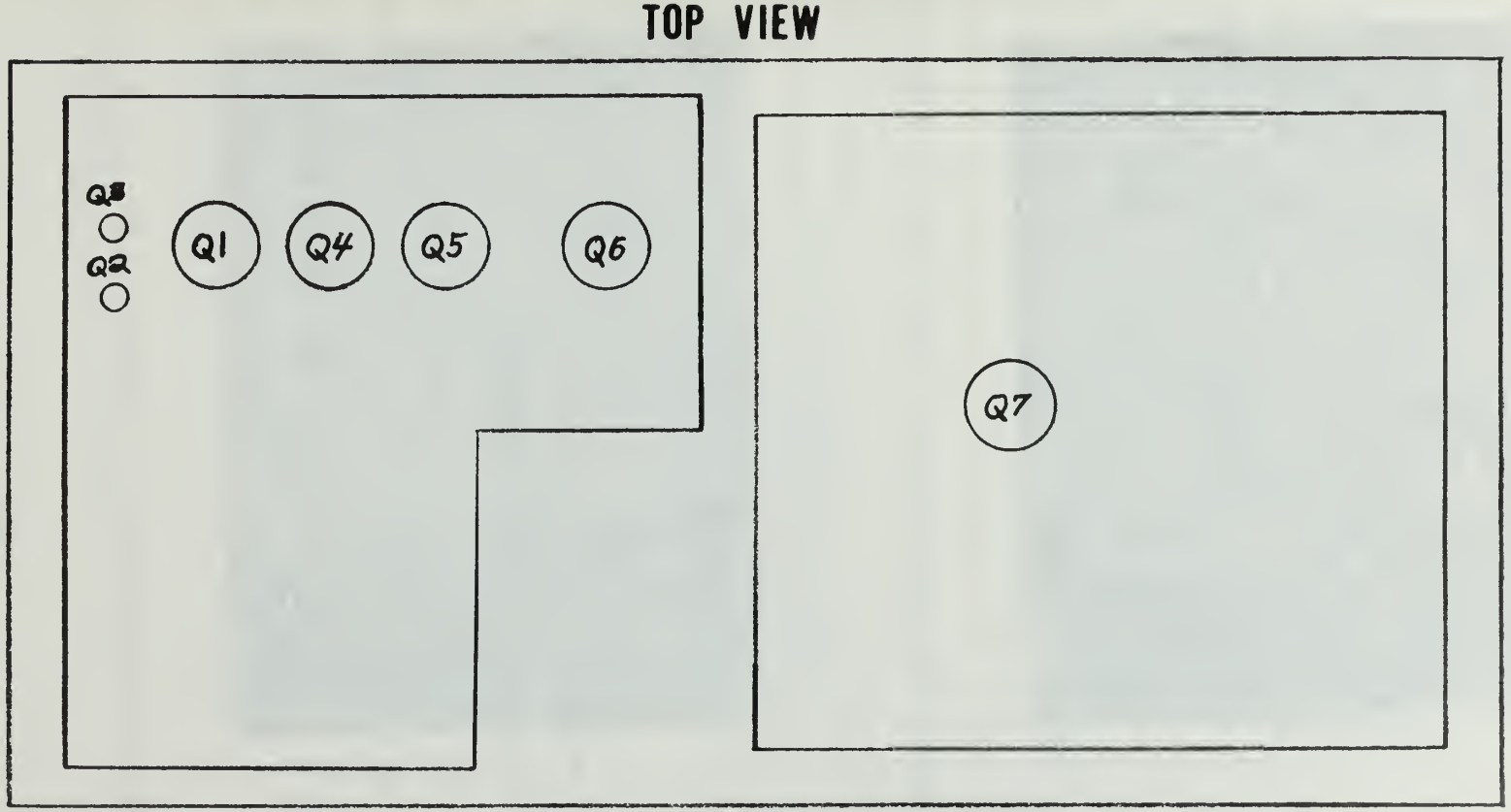


FIGURE 20 RADIOSONDE MODULATOR AND TRANSMITTER OVERALL SCHEMATIC



MODULATOR-TRANSMITTER TRANSISTOR LAYOUT

FIGURE 21

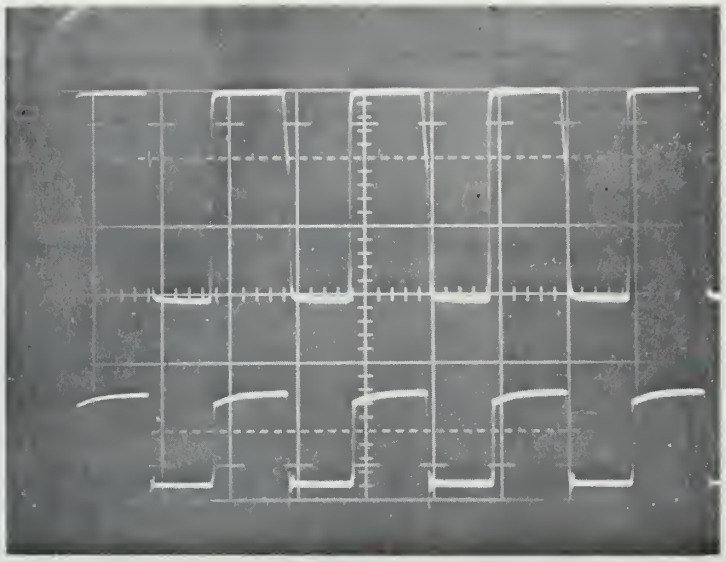


FIGURE 22 CARRIER ENVELOPE AND SWITCHING WAVEFORMS-LOW PRF

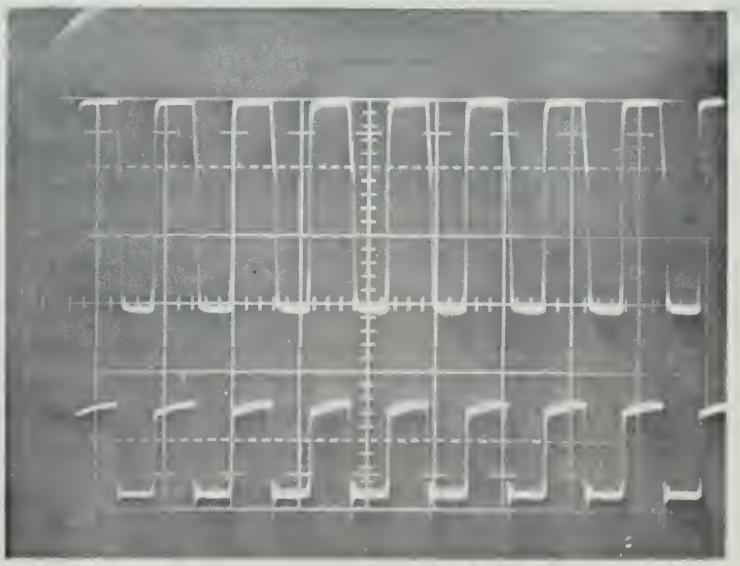


FIGURE 23 CARRIER ENVELOPE AND SWITCHING WAVEFORMS-HIGH PRF

V. SYSTEM OPERATIONAL RESULTS

The multiplexer was connected to the modulator-transmitter. A variable voltage source was connected to the inputs of S1 through S6. The input to S8 was grounded. The output of the multiplexer controls the frequency out of the VCM which in turn triggers the power oscillator. Fig. 24 is a photograph of the 400MHz RF envelope. The sweep speed is 500 milliseconds per centimeter. The top trace is the switching waveform on the collector of Q6(Fig. 16), and the bottom trace is the detected transmitter carrier envelope. Note that three multiplexer cycles appear on each trace. Increasing the sweep produces the same waveforms as shown in Figs. 22 and 23. Fig. 25 is a photograph of the transmitter spectrum. The PRF of the transmitter was 80 KHz. The center lobe width is 320 KHz. between minimums as anticipated.

A. SYSTEM ENVIRONMENTAL TESTS

The multiplexer and modulator/transmitter as shown in Figs. 26(a) and (b) were placed in a chamber and subjected to temperatures from +75°C to -70°C. The VCM output, transmitter power, and transmitter frequency were monitored as the simulated input sensor voltages to the multiplexer were varied from minus five to minus ten volts. The results of these tests are given below.

1. Power Output

At 20°C the peak power output of the transmitter was 5.9 watts. The average power was

$$\frac{1}{8}(5.9) = 737 \text{ milliwatts}$$

note: Duty Cycle = $\frac{1}{8}$

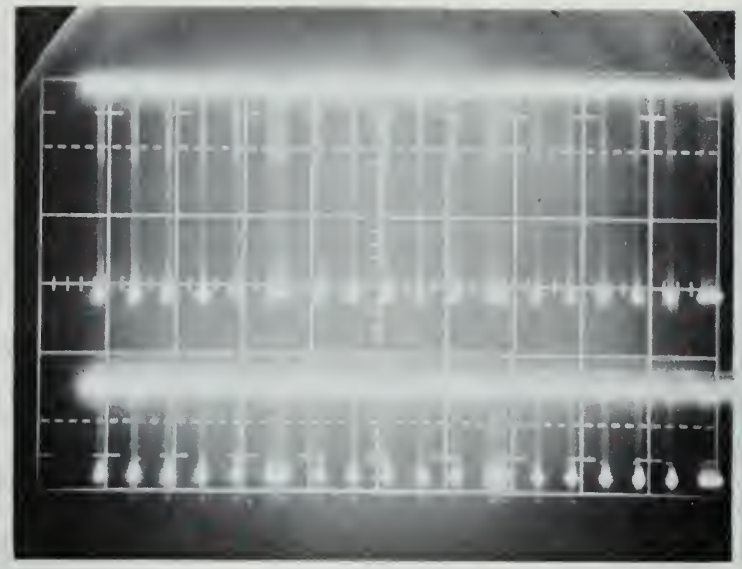


FIGURE 24 CARRIER ENVELOPE AND SWITCHING WAVEFORMS-SLOW SWEEP

FIGURE 25 EXPERIMENTAL TRANSMITTER FREQUENCY SPECTRUM

The system was then placed in an environment chamber. It should be noted that the power transistor did not have a heat sink attached throughout the tests described in this section. In addition, the entire system was left open to the environment. Under actual operation the system would be enclosed in a container which would provide some degree of protection from the elements. The power output measurements obtained over the temperature range is shown in Table 2.

Temp. (°C)	Peak Power (Watts)
75	5.5
60	5.5
45	5.6
30	5.7
15	6.0
0	6.0
-15	6.0
-30	6.2
-45	6.3
-60	6.3
-67	6.3

TABLE 2

At -67°C the transmitter became intermittent. Investigation revealed that Q5 (Fig. 20) was not providing enough drive to Q6. The loss of current gain at this temperature prevented Q5 from functioning properly.

The operating temperature range of the power oscillator was extended from -30°C to -70°C with the addition of C3 (Fig. 19). When Q6 is turned on the voltage on the base of the power oscillator lags the negative going emitter voltage long enough to provide the forward

FIGURE 26a PHOTOGRAPH OF RADIOSONDE SYSTEM

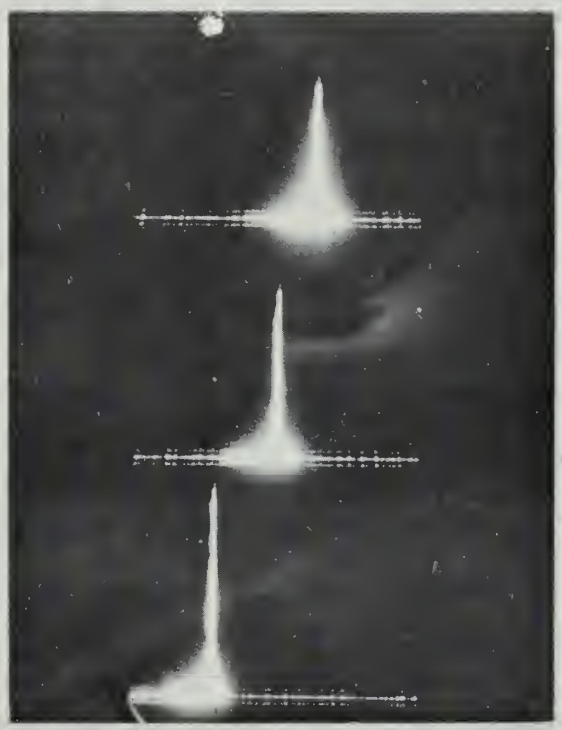


FIGURE 27 TRANSMITTER FREQUENCY DRIFT

VOLTS	FREQ(KHz)			FREQ(KHz)			FREQ(KHz)		
	Run 1	Run 2	Run 3	Run 1	Run 2	Run 3	Run 1	Run 2	Run 3
	T = 75°C			T = 30°C			T = -15°C		
-5	38.079	37.919	37.880	37.225	37.125	37.085	35.383	35.481	35.305
-6	46.859	46.627	46.628	45.818	45.835	45.731	43.757	43.913	43.715
-7	55.823	55.597	55.552	54.682	54.630	54.529	52.267	52.492	52.176
-8	65.066	64.696	64.672	63.710	63.623	63.515	60.895	61.160	60.767
-9	74.535	74.082	74.029	72.912	72.826	72.698	69.665	69.957	69.523
-10	83.860	83.866	83.785	82.417	82.243	82.078	78.645	78.939	78.486
	T = 60°C			T = 15°C			T = -30°C		
-5	37.868	37.683	37.720	36.695	36.663	36.567	34.892	34.827	34.726
-6	46.548	46.463	46.421	45.351	45.297	45.144	43.175	43.109	43.008
-7	55.510	55.357	55.374	54.077	54.035	53.901	51.566	51.504	51.400
-8	64.600	64.415	64.446	63.044	62.932	62.770	60.122	60.034	59.864
-9	74.010	73.786	73.774	72.116	72.003	71.817	68.780	68.685	68.511
-10	83.570	83.366	83.390	81.388	81.298	81.089	77.544	77.502	77.310
	T = 45°C			T = 0°C			T = -45°C		
-5	37.420	37.457	37.420	36.146	36.107	36.000	34.053	34.046	33.970
-6	46.229	46.204	46.116	44.661	44.618	44.528	42.229	42.165	42.090
-7	55.166	55.075	54.997	53.276	53.270	53.096	50.449	50.424	50.272
-8	64.189	64.137	64.030	62.095	62.050	61.867	58.843	58.743	58.619
-9	73.468	73.395	73.271	71.076	71.008	70.821	67.222	67.161	67.064
-10	83.045	82.692	82.792	80.240	80.212	79.989	75.844	75.713	75.618
	T = -60°C			T = -67°C					
-5	33.160	33.171	33.039	32.790	32.781	32.680			
-6	41.157	41.135	40.990	40.620	40.569	40.472			
-7	49.146	49.128	49.009	48.520	48.487	48.361			
-8	57.264	57.267	57.105	56.580	56.487	56.356			
-9	65.530	65.465	65.288	64.640	64.621	64.423			
-10	73.833	73.770	73.580	72.838	72.826	72.570			

TABLE 3

the location of the crossover points for each curve from negative to positive (and VIS-A-VIS) deviations being relatively constant.

To investigate the possibility that a second order approximation would better fit the VCM data another computer run was made. Fig. 30 shows the second order approximations at the temperatures indicated. Fig. 31 shows the deviation of the experimental data from the second order curves. The deviations appear to be more random, but more important is the fact that the deviations have been reduced significantly. The maximum positive and negative deviations appear to be approximately 30 Hz and 60 Hz respectively with an average of approximately 20 Hz.

Appendix E lists the computer printout for the case of the second order approximation. The variable Y(I) represents the coefficients of the polynomial

$$A + Bt + Ct^2 = EZ$$

The variable EZ is the frequency of the least square fit plotted for each value of I where I = -3,-2,-1,0,1,2, and the conversion for the VCM input voltage (V_{in}) is:

$$V_{in} = -(8 + I) \text{ volts}$$

On the calplot outputs (Figs. 28 through 31) the horizontal scale has been shifted to the left five units so that the origin represents a VCM input of -5 volts and increasing to the right to -10 volts. The vertical scale for the least square estimation plots are equal to 30 KHz + (vertical X 10) KHz while those of the deviation plots are (vertical X 10) Hz.

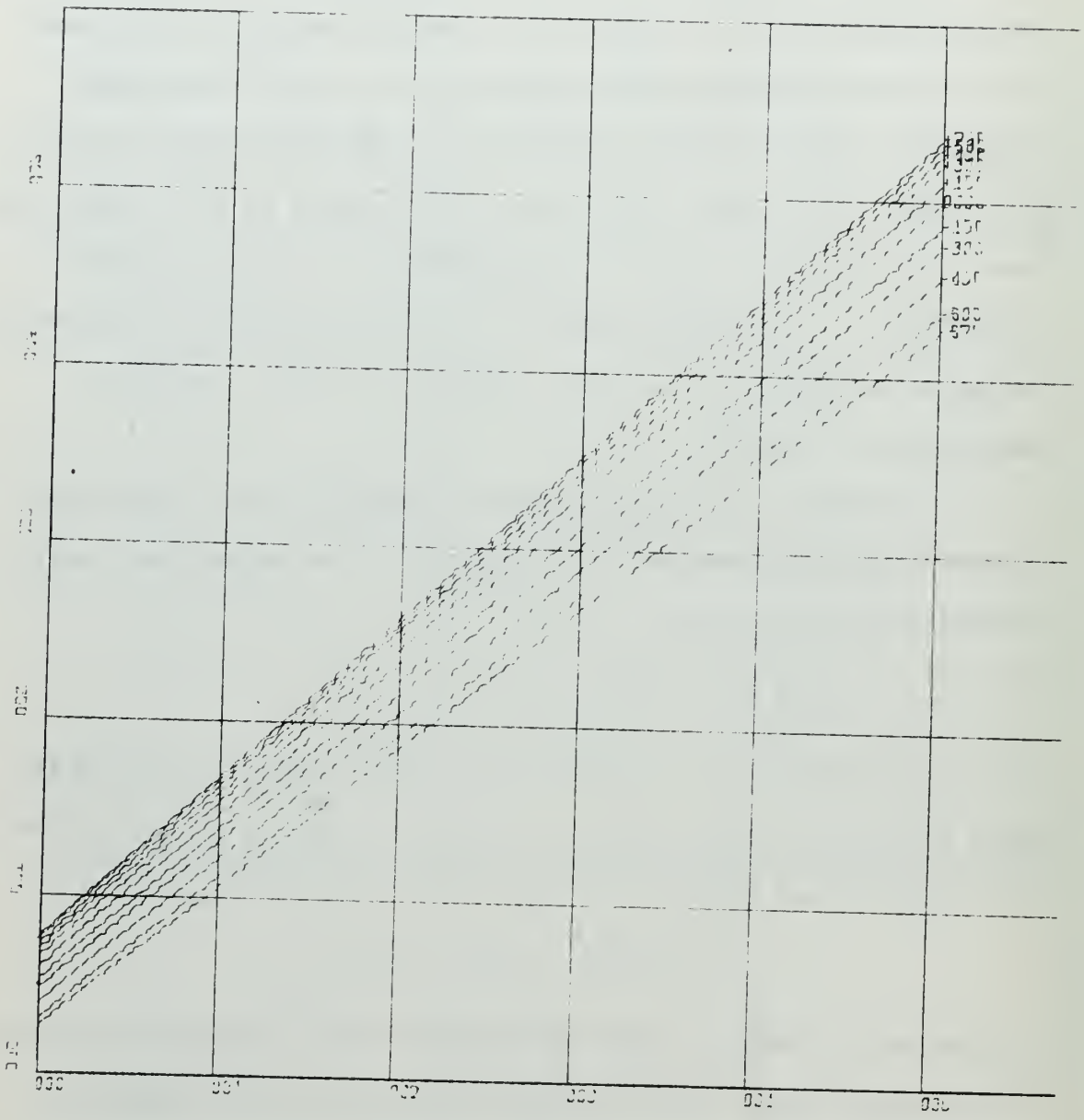


FIGURE 28 FIRST ORDER APPROXIMATIONS OF VCM DATA

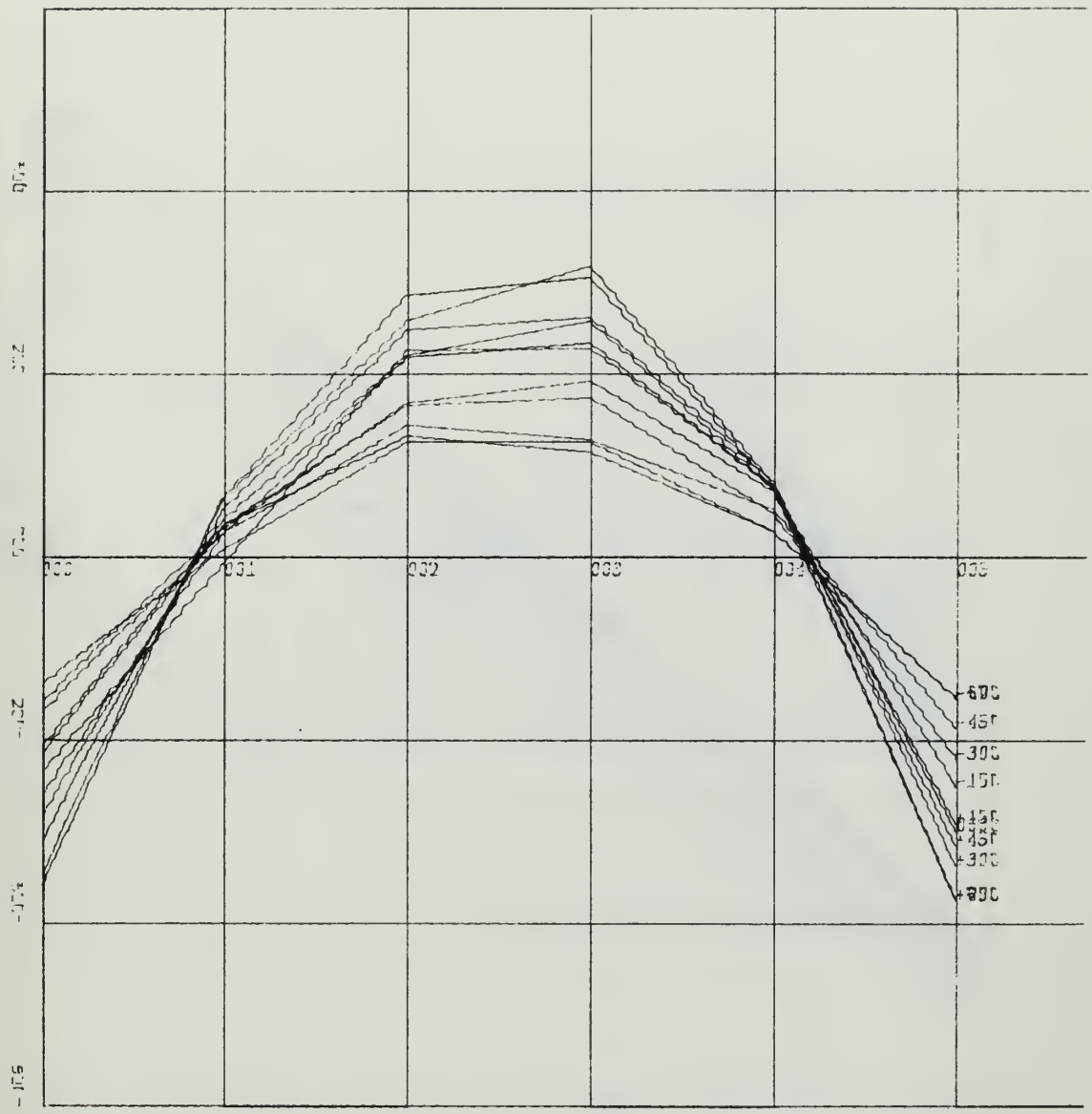


FIGURE 29 DEVIATION OF DATA FROM FIRST ORDER APPROXIMATIONS

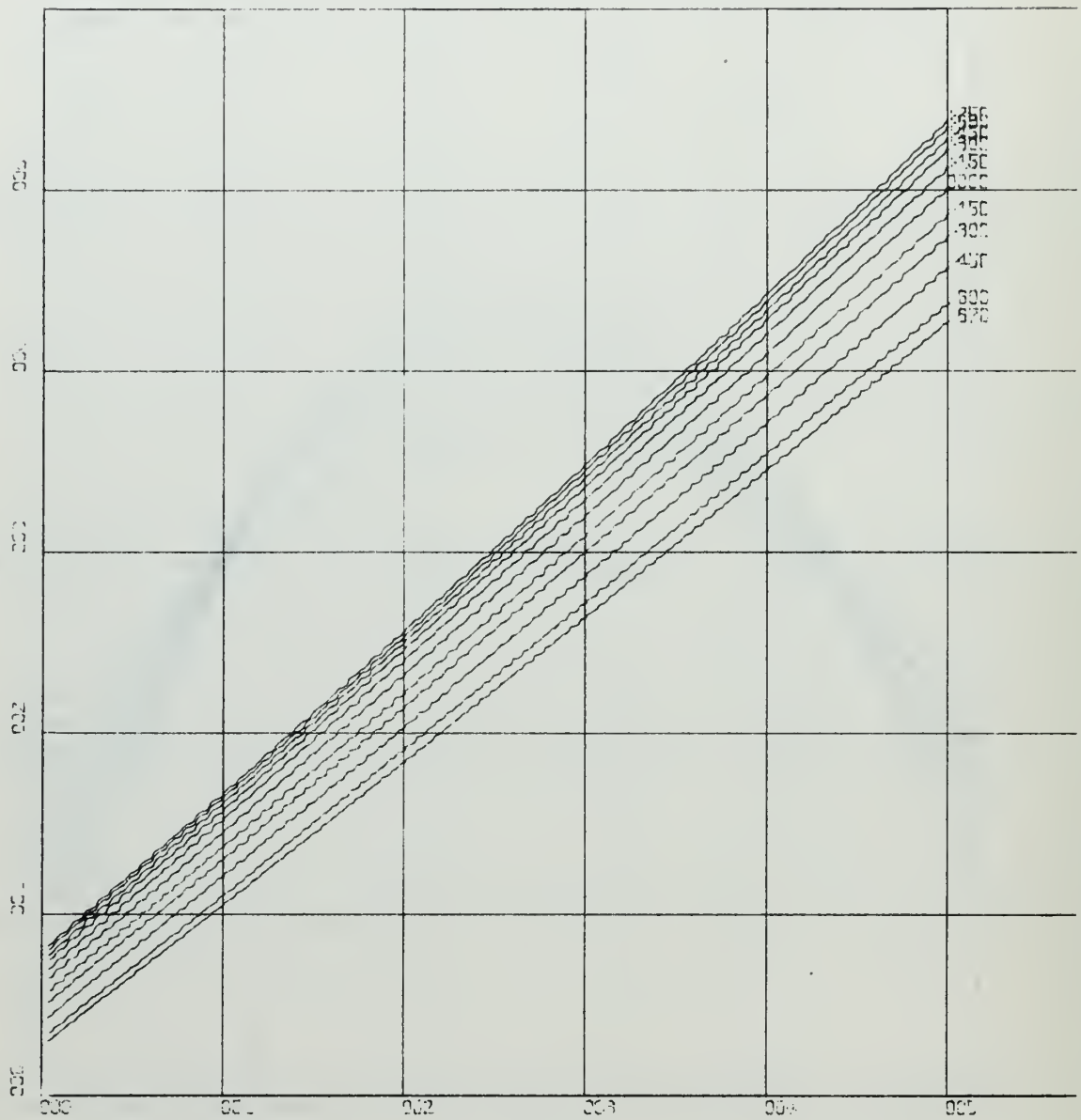


FIGURE 30 SECOND ORDER APPROXIMATIONS OF VCM DATA

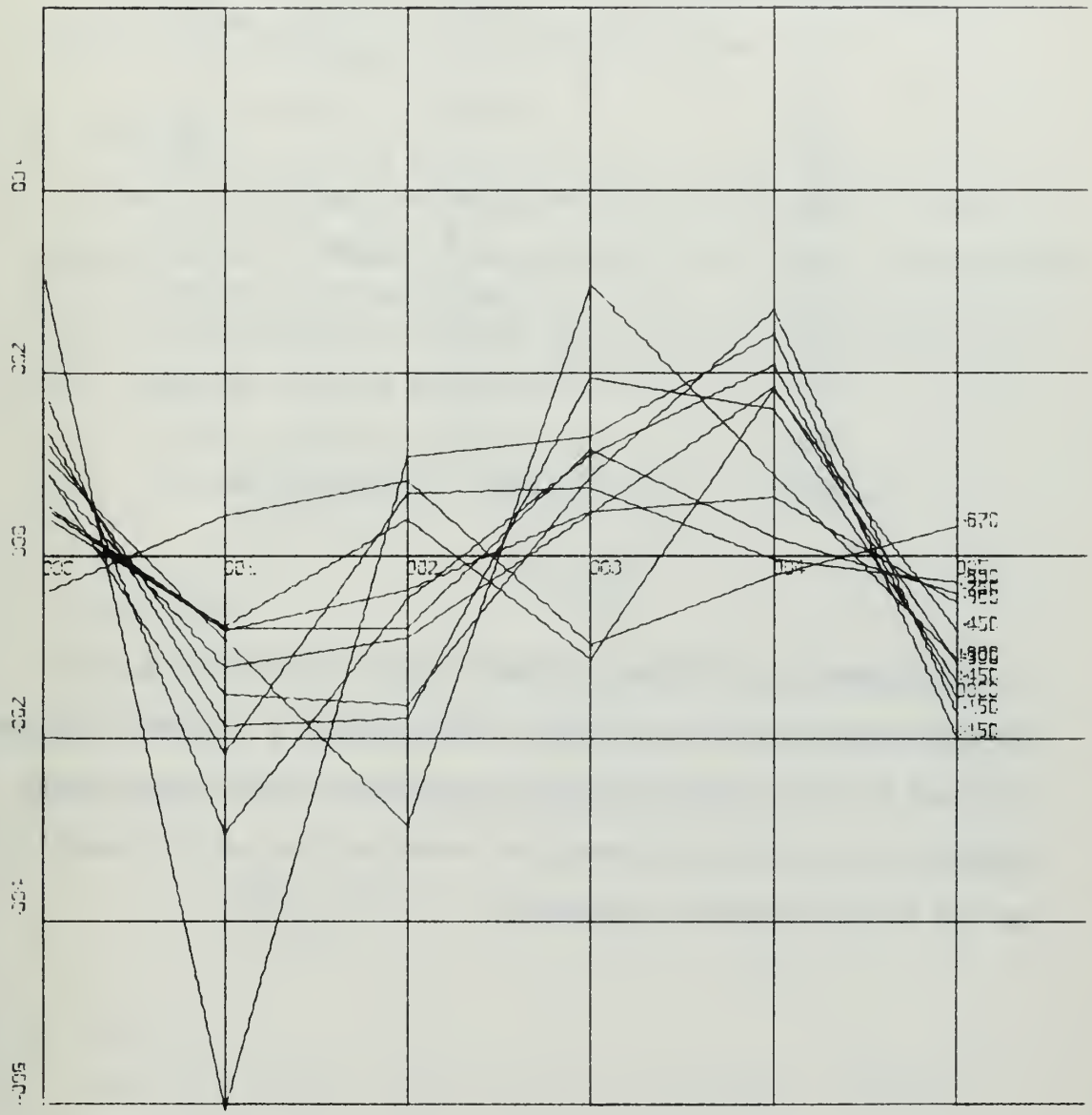


FIGURE 31 DEVIATION OF DATA FROM SECOND ORDER APPROXIMATIONS

The equations of the second order approximations are given in Table 4.

TEMPERATURE (°C)	EQUATIONS f in KHz, V = - (I + 8) volts
75	$f = .110I^2 + 9.284I + 64.823$
60	$f = .108I^2 + 9.240I + 64.516$
45	$f = .089I^2 + 9.166I + 64.138$
30	$f = .096I^2 + 9.112I + 63.620$
15	$f = .081I^2 + 8.993I + 62.928$
0	$f = .084I^2 + 8.889I + 62.015$
-15	$f = .069I^2 + 8.723I + 60.949$
-30	$f = .064I^2 + 8.589I + 60.011$
-45	$f = .053I^2 + 8.390I + 58.723$
-60	$f = .045I^2 + 8.163I + 57.219$
-67	$f = .047I^2 + 8.047I + 56.464$

TABLE 4

It can be seen that although the coefficients of the second order approximations are relatively small, they cannot be ignored. Much more data must be taken and analyzed more completely before any definite statements can be made regarding the predictability of the behavior of the VCM in this type of environment.

VI. DATA RESOLUTION

The theoretical resolution of the information received from the radiosonde is determined in the following manner.

A. PRESSURE

Assuming the output voltage from the pressure sensor network at 1060 mb pressure is -10 volts and at 5 mb, is -5 volts. For the VCM, the output frequency, f_o, for -10 volts input is 80 KHz, and for -5 volts input, is 37 KHz. The resolution is:

$$\frac{(10-5)\text{ volts}}{(1060-5)\text{ mb}} \times \frac{(80-37)\text{ KHz}}{(10-5)\text{ volts}} = 41\text{ Hz/mb}$$

B. TEMPERATURE

Assuming the same output voltage range for the temperature sensing network as obtained from the pressure network for a temperature range of +70° C to -70° C, the resolution is:

$$\frac{(80-37)\text{ KHz}}{(70+70)\text{ °C}} = 307\text{ Hz/°C} = 30.7\text{ Hz/.1° C}$$

C. HUMIDITY

Assuming the same voltage outputs as above for a measured humidity range of 10% to 90%. The resolution is:

$$\frac{(80-37)\text{ KHz}}{(90-10)\text{ \%}} = 537\text{ Hz/1\% humidity}$$

$$= 53.7\text{ Hz/.1\% humidity}$$

VII. SYSTEM WEIGHT

If it is assumed that there will be no change in the weight of the radiosonde battery (AMT-4A), the approximate weight of the solid state system is:

Battery	500 grams
Modulator and transmitter	100 grams
Total weight	600 grams

This weight includes only the electronics package. The reduction in weight over the present system is

$$\frac{1103-600}{1103} \times 100 = 45.6\%$$

where the AMT-4A weight is given as 1103 grams. The modulator and transmitter weight shown above is double the actual weight of the breadboarded device. The additional 50 grams were added to account for the additional weight of sensors and associated circuitry. This added weight is considered more than sufficient to cover these additional components.

The weight reduction shown above is an approximation. However, the author feels that it is realistic because of the assumption of no change in battery weight. Since a reduction in physical size is also going to be realized then it must be assumed that some weight savings must result from the system packaging. In any event, the assumption made above, if anything, is conservative.

VIII. SYSTEM COST

Only those parts of the electronics system considered significant will be discussed. Cost of components such as resistors and capacitors will not be covered.

A. LSI MULTIPLEXER

A cost analysis was made by comparing chip size, market requirements, and circuit complexity with similar chips presently on the market. The cost is based on a 1971 market. Table 5 is a list of the standard cells required to implement the multiplexer shown in Fig. 15. The components required to include the crystal oscillator are also listed.

Standard Cell[1]	Total used	Total length in mils
FRS2	25	275
CG	2	32
NAND3	2	8
NAND2	3	12
GA4	3	18
NOR4	2	10
OUT	6	36
NOR2	6	18
NOR3	1	4
NREX3	1	3
PD	9	18
	TOTAL	434

Crystal Oscillator Components	Area in Square mils
240 kilohm resistor	20
68 " "	5
12 " "	3
22 " "	6
30 pf capacitor	150
Q1 MOS-FET	10
Q2 MOS-FET	10
TOTAL	204

TABLE 5

[1] Fairchild's standard cell notation

The multiplexer chip size is determined in the following manner:

Area of each cell = (L X 8) $mils^2$ = A_c

where L = length of the cell

Total active area of the cell = 2 X A_c

Then the total length of each side of the chip is:

$$L_T = \sqrt{2A_c} = \sqrt{16L} = 4\sqrt{L}$$

To account for the pads, 11 mils must be added

$$L_T = (11 + 4\sqrt{L}) \text{ mils}$$

The total length including the oscillator is:

$$L_T = 4\sqrt{434} + \sqrt{204} + 11 \text{ mils}$$

$$= 94.2 + 14.3 = 108.5 \text{ mils}$$

A custom, handcrafted layout would reduce the size of the chip by at least 20% to approximately 87 mils. The number of external pin connections required on the chip package is 13, so a basic 16 pin dual in-line package could be used. Compared to present costs, such a device could be sold at less than five dollars each. This, of course, is also based on the high usage this device would have.

B. POWER TRANSISTOR

The device used is not presently on the market and no definite cost could be determined. The device is packaged in a stripline configuration and the cost of these are quite significant. During the power oscillator design it was shown that no heat sink would be required because of the low duty cycle. This fact eliminates the need for the expensive package. Also discussed was the possibility of reducing the power requirements on the radiosonde. Based on the last two items the author feels that a long range estimate of the cost of the high frequency power transistor would be approximately four dollars

each. With high frequency power transistor technology advancing as rapidly as it is at the present time there is no reason to believe that the cost given above is unrealistic.

C. MODULATOR

All transistors used in this section are low cost, epoxy types except for the switching transistor Q6 (see Fig. 20). The author feels that the entire modulator, including the crystal in the multiplexer clock and all other basic components could be assembled at an overall cost of under six dollars.

D. METEOROLOGICAL SENSORS

This area was not covered by this thesis and no estimation of costs will be given.

E. COST CONCLUSIONS

The costs shown above are only approximations. They are included only to indicate that the cost of a solid state radiosonde will not be too high to render it impractical as an expendable device. It should be reemphasized that from such a system we can expect:

(1) improved data accuracy

(2) increased channel capacity

(3) increased data rate

(4) increased reliability

(5) decrease in weight

(6) decrease in size

which is a good argument for implementing a solid state system.

IX. INTERFACING CONSIDERATIONS

System interfacing with meteorological sensors and the reduction of data at the terminal installation are considered in this section. No actual interfacing was performed in the laboratory. All the information contained below is included to assist those who would continue the work started in the thesis.

A. METEOROLOGICAL SENSORS

Present common radiosonde sensors are of the resistance type. Pressure sensor of the voltage type are also available. The following are possible interface networks for such devices.

Resistance — Fig. 32 shows a configuration which could be used to obtain the desired VCM input. R_X is the meteorological sensor and the output voltage, V_o, is determined by the voltage divider network.

Voltage — A simple operational amplifier, if required, could provide the required input voltages to the VCM.

An example network is shown in Fig. 33. The ratios $\frac{R2}{R1} = \frac{R4}{R3}$ (amplifier gain) and the -5 volt input would set the output voltage at -5 volts with zero input voltage and determine the range of the output voltage for a given input range. Q is an operational amplifier such as the Fairchild 741.

B. RADIOSONDE RECEIVER OUTPUT

It is desirable to either connect the receiver output directly to a computer or to transform the output to a digital format for direct relay to a central computer system. In either case, the reduction of

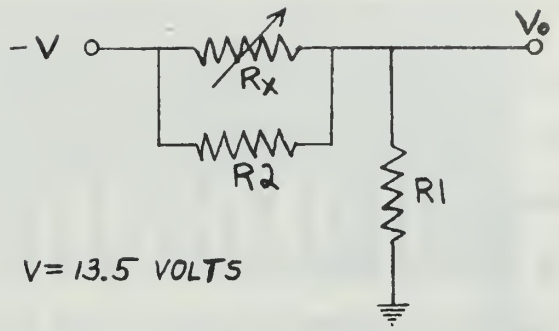


FIGURE 32 RESISTANCE SENSOR INTERFACE CIRCUIT

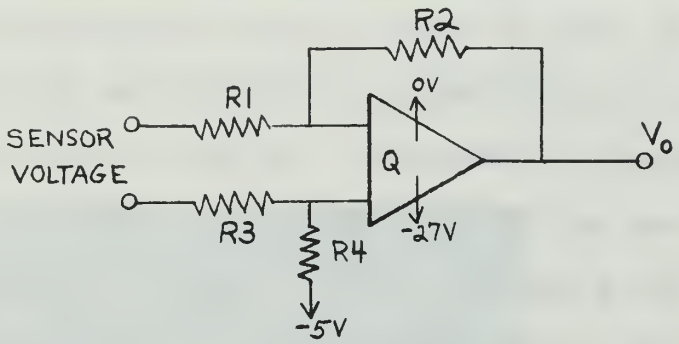


FIGURE 33 VOLTAGE SENSOR INTERFACE CIRCUIT

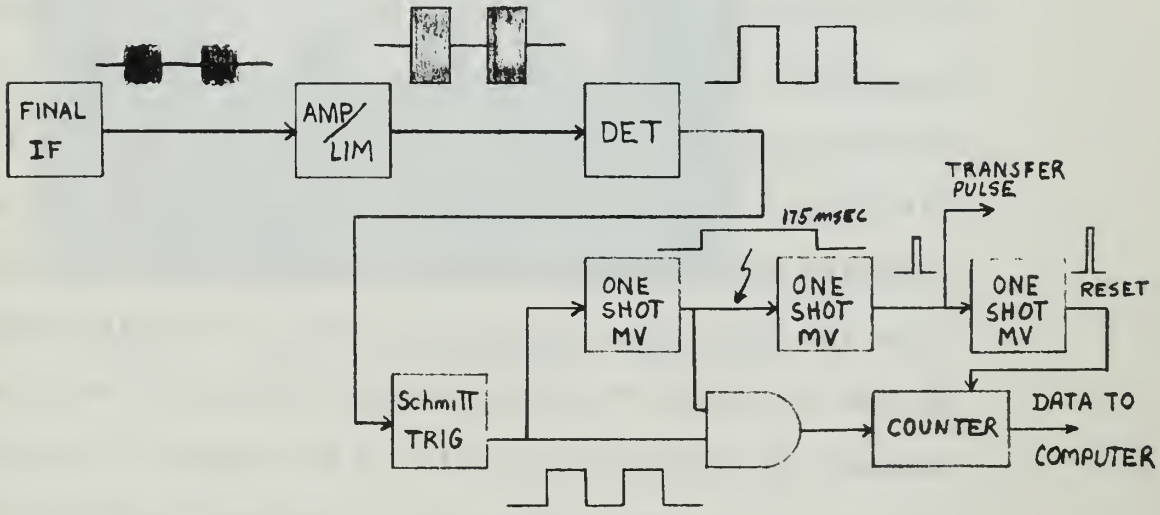


FIGURE 34 RECEIVER DECODING NETWORK

raw data to meteorological information would be accomplished automatically without the introduction of human errors or loss of accuracy due to analog to digital transformations.

The SMQ-1A Radiosonde Receiver was used to determine whether the signal transmitted by the breadboarded system would be reproduced sufficiently to allow detection and subsequent decoding. Throughout the design stages, consideration was given to the receiver characteristics in order that few modifications would be required to have the receptor work with the experimental radiosonde. Figs. 35 and 36 are actual photographs taken at the output of the final IF stage in the SMQ-1A. Fig. 35, taken at a very slow sweep speed, clearly shows the time multiplexed sequence. Fig. 36 shows the GVPRF signal. The IF frequency is 22 Megaherts. The peak to peak voltage shown is 1.5 volts.

From the results of the test with the SMQ-1A, it is seen that the PRF can be measured by using a simple AM detector and logic to count and either store or transfer the information to the computer. Fig. 34 depicts a possible network to accomplish this task. The output of the IF is fed to an amplifier-limiter stage. The amplifier output is then detected and fed to a Schmitt trigger whose threshold is set above the incoming noise leve. The Schmitt trigger output is fed to a One-Shot multivibrator which generates a 175 millisecond pulse. The data pulses, along with the Schmitt trigger output, are fed to an AND gate which allows the data pulses to be counted for up to 175 milliseconds. When the gate is turned off a second One-Shot generates a short pulse which transfers the data from the counter to the computer. At the completion of the transfer another short pulse is generated which clears the counter for the next set of input data.

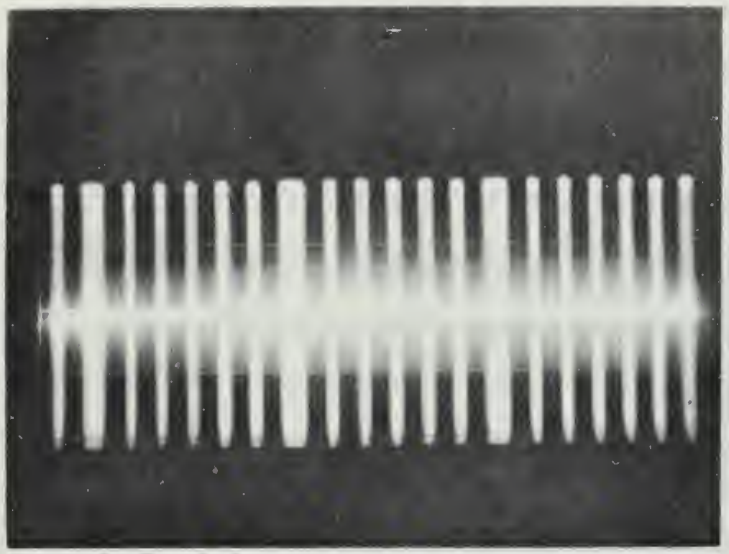


FIGURE 35 RECEIVER IF WAVEFORM - SLOW SWEEP

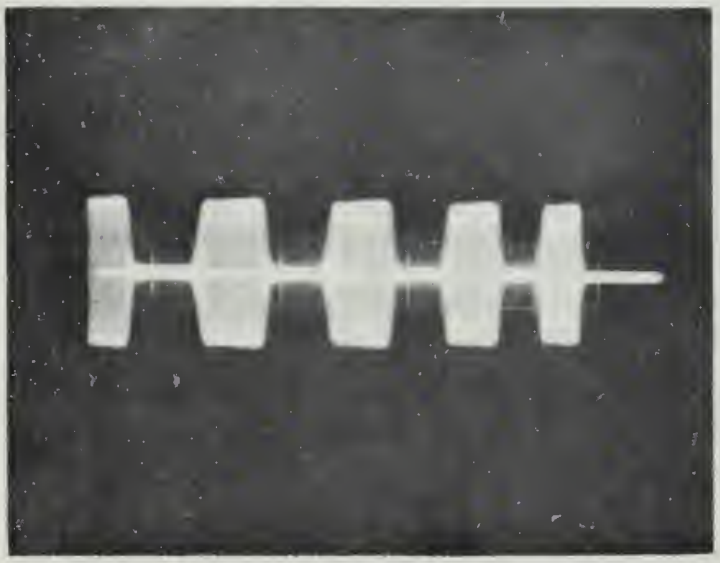


FIGURE 36 RECEIVER IF WAVEFORM - FAST SWEEP

The calibration pulse is detected easily by noting the large pulse count. This can be programmed directly into the computer. The 175 millisecond gate allows the calibration pulses to be counted for the entire 150 milliseconds. Since there are 250 milliseconds between channels, the time available to transfer the information to the computer and clear the counter is 75 milliseconds. The circuit in Fig. 35 was not fabricated, however, there is reason to believe that the concept is sound and practical.

X. CONCLUSION

This thesis dealt primarily with the feasability of designing and building a complete solid state radiosonde. Throughout the entire period of development, cost, complexity, size, weight, compatability with present ground receptors, data accuracy, RF power output, bandwidth, etc., were the determining factors in the overall design. State-of-the-art technology was used wherever possible. Although no testing was done with actual meteorological sensors, a great deal of thought was given to the types of sensors which might be used.

Fig. 37 shows a typical overall system, including sensors. Depicted are resistance type humidity and temperature sensors while the pressure sensor is a bridge type (lower left) requiring a constant current source. An amplifier is required to bring the voltage up into the VCM input range. The eight volt input reference for the calibration/sync period is obtained from this network. This circuit was actually built and operated satisfactorily. The transistor shown, without a base lead, is a Fairchild SE 2001 which, when operated in a reverse zener breakdown mode, provides a constant output voltage which is relatively independent of temperature. Not shown in the diagram is the logic circuits which drive the MOS analog switches.

The operational testing done on the system showed that the system performed satisfactorily over a wide range of temperatures. Test periods lasted up to six hours with no failure occuring in any part of the system. All tests were made without the advantage of any protective covering over the chassis. Concern over the possibility of the epoxy transistors failing at low pressures due to rupturing of the package

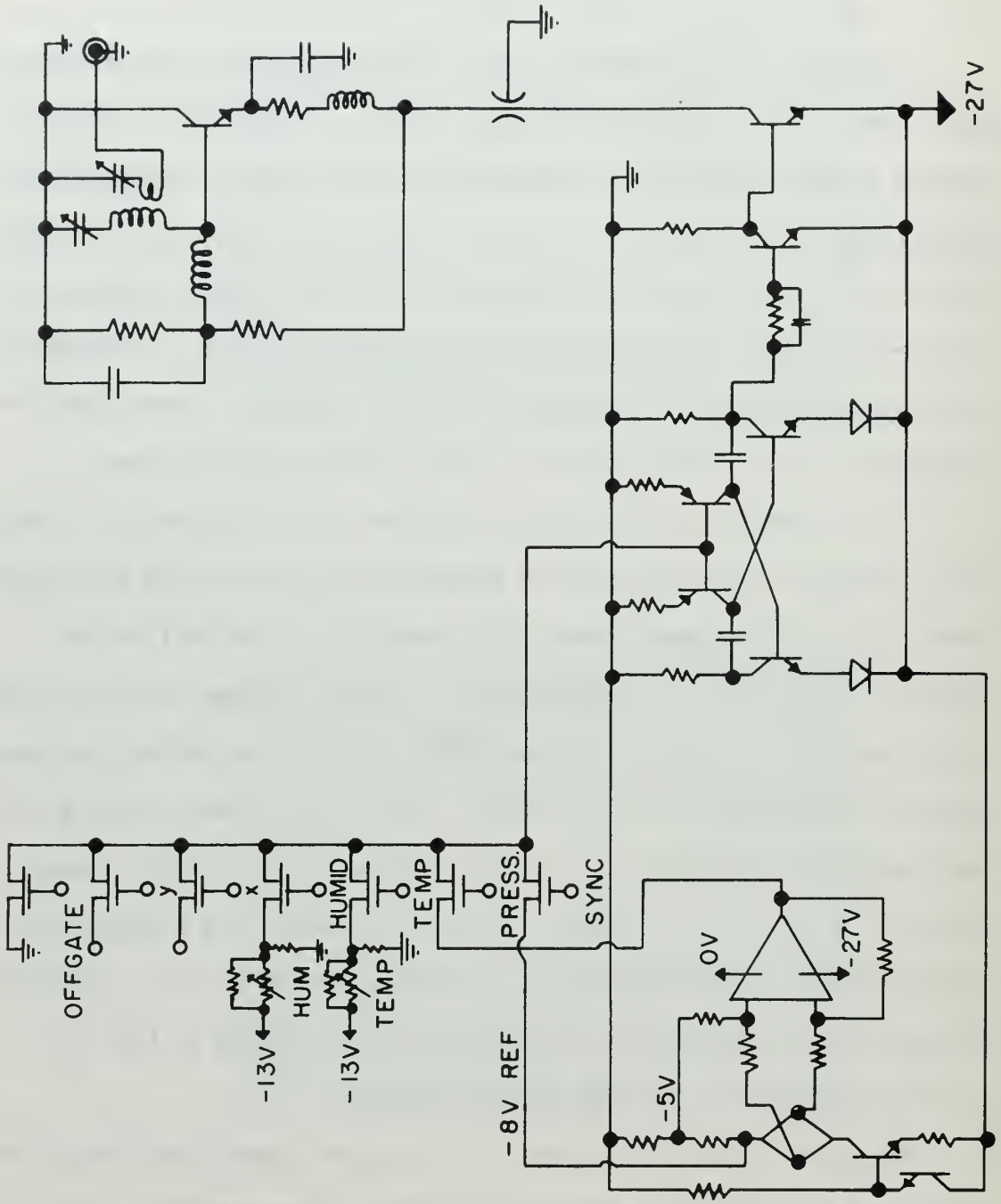


FIGURE 37 OVERALL RADIOSONDE SCHEMATIC DIAGRAM

proved to be incorrect. Several transistors of various types were taken down to as low as one millibar without failing. Therefore, it appears that the entire system is capable of functioning properly over any of the adverse conditions to which the radiosonde is subjected.

MOS technology has allowed LSI to become more efficient and reliable. Of equal importance is the cost reduction. The MOS/LSI Multiplexer design not only improves the data rate and channel capacity, but significantly decreases the size and weight of the system. The simulated multiplexer, which was built of discrete MOS IC's, also performed satisfactorily under adverse environmental testing. In fact, the multiplexer continued to function at temperatures below -70° C even after the rest of the system had ceased to operate reliably.

Analysis of the VCM over variable voltage and temperature conditions showed that a second order curve could be fitted to the output data. Errors resulting from this approximation are less than .1% and, on the average, less than .03%. A linear approximation provides errors of less than 1.25%. The reduction of data by a computer appears to be feasible and further investigation of this phase of operation could be the topic of another thesis.

The results obtained through this thesis appear to favor the development and use of a solid state radiosonde. Generally speaking, nothing was found which might show the superiority of the present system over a new system. The only area which may favor the present radiosonde is cost. But the advantages gained by the solid state system far outweigh, in the author's estimation, any additional costs. The author also feels that the cost differential would rapidly decrease as production techniques are improved on the present state-of-the-art components.

APPENDIX A CAD SIMULATION PROGRAM

```
STMT      SOURCE STATEMENT

    1             MACRO
    2   &Z        MCD     &A1,&A2,&B1,&B2,&B3,&C1,&DEL
    3   &Z.2      NAND3   &B1,&B2,&B3,&DEL
    4   &Z.4      NAND2   &A1,&A2,&DEL
    5   &Z.5      NAND3   &B2,&B3,&C1,&DEL
    6   &Z.6      NAND2   &A2,&Z.2,&DEL
    7   &Z.7      NAND2   &Z.4,&Z.5,&DEL
    8             MEND
    9             MACRO
   10   &X        SHREG   &M1,&M2,&N1,&N2,&CLOCK,&CLOCKN,&DEL
   11   &X.1      GA4     &M1,&M2,&N1,&N2,1
   12   &X.2      FRS2    &X.11,&CLOCK,&CLOCK,&X.12,CD,&CLOCKN,1
   13             MEND
   14             MSMCSAIC
   15             NETSTART
   19   T15Q      CG      IN,1
   61   FST       MCD     PE1,LG,SR1QN,PE1N,SR42QN,SR1Q,1
  171   SR1       FRS2    FST6,T15Q,T15Q,FST7,CD,T15QN,1
  269   SR2       SHREG   LC,PE1,PE1N,SR1QN,T15Q,T15QN,1
  407   SR3       SHREG   SR5Q,PE1,PE1N,SR22QN,T15Q,T15QN,1
  545   SR4       SHREG   SR5Q,PE1,PE1N,SR32QN,T15Q,T15QN,1
  683   PE1       NCR4    SR1Q,SR22QN,SR32Q,SR42QN,1
  709   PE1N      NCR2    PE1,ZERO,0
  731   PE2       NOR2    SR32QN,SR42QN,1
  753   FP        OUT     PE2,CD,1
  780   CL2       NCR4    SR1QN,SR22Q,SR32QN,SR42Q,1
  806   CP2       CG      CL2,1
  848   G5        OUT     PE2,SR10QN,1
  875   SR5       FRS2    G51,CP2,CP2,G52,FP1,CP2N,1
  973   G6        OUT     PE2,SR5QN,1
 1000   SR6       FRS2    G61,CP2,CP2,G62,FP1,CP2N,1
 1098   G7        OUT     PE2,SR6QN,1
 1125   SR7       FRS2    G72,CP2,CP2,G71,FP1,CP2N,1
 1223   G8        OUT     PE2,SR7QN,1
 1250   SR8       FRS2    G82,CP2,CP2,G81,FP1,CP2N,1
 1348   G9        OUT     PE2,SR8QN,1
 1375   SR9       FRS2    G92,CP2,CP2,G91,FP1,CP2N,1
 1473   G10       OUT     PE2,SR9QN,1
 1500   SR10      FRS2    G102,CP2,CP2,G101,FP1,CP2N,1
 1598   CLGATE    NAND2   CP2N,SR42Q,1
 1620   YOUT      NCR2    SR10QN,CLGATE,1
 1642   XOUT      NCR2    SR9QN,CLGATE,1
 1664   HOUT      NCR2    SR8QN,CLGATE,1
 1686   TOUT      NCR2    SR7QN,CLGATE,1
 1708   POUT      NCR2    SR6QN,CLGATE,1
 1730   SYNOUT    NCR2    SR5Q,CLGATE,1
 1752   EXNOR     NREX3   XOUT,YOUT,HOUT,OFFGATE,1
 1783   OFFGATE   NCR3    TOUT,POUT,SYNOUT,1
 1807             NETEND
```

FAIRCHILD MACROLOGIC SIMULATION PROGRAM - - COMPILATION PHASE

```
STMT. NO.    SIMULATION CONTROL PROGRAM STATEMENT

  0001               P OFFGATE,,SYNCLT,,POUT,,TCUT,,HCUT,,XCUT,,YCUT
  0002               PE 30
  0003               PT 'FIVE CHANNEL MULTIPLEXER OUTPUT'
  0004               ST 01 ZERO,LO
  0005               S 1 (25) CD
  0006               S 0 (15,30,ETC.) IN
  0007               SU TIME=6000
  0008               F
```

NO APPARENT ERRORS IN ABOVE SIMULATION CONTROL PROGRAM

APPENDIX B CAD SIMULATION PRINTOUT

TIME		OFFGATE	SYNOUT	PCUT	TCUT	HOUT	XOUT	YOUT
000000	*							
000030	*	1	C	C	C	C	C	0
000060	*	1	0	0	C	0	0	0
000090	*	1	C	C	0	C	C	0
000120	*	1	0	0	C	0	C	0
000150	*	0	0	1	0	0	C	0
000180	*	1	0	C	0	0	0	0
000210	*	1	C	C	C	0	0	0
000240	*	1	C	0	0	0	0	0
000270	*	1	C	C	0	C	0	0
000300	*	0	0	0	1	C	0	0
000330	*	1	0	C	0	C	C	0
000360	*	1	0	0	0	C	C	0
000390	*	1	C	0	C	C	0	0
000420	*	1	C	0	C	C	C	0
000450	*	0	0	0	0	1	C	0
000480	*	1	0	0	C	0	0	0
000510	*	1	C	0	0	C	C	0
000540	*	1	0	C	0	C	C	0
000570	*	1	C	C	C	C	0	0
000600	*	0	C	0	0	0	1	0
000630	*	1	C	C	0	C	C	0
000660	*	1	C	0	0	0	0	0
000690	*	1	0	0	C	C	C	0
000720	*	1	0	C	0	C	C	0
000750	*	0	C	C	0	C	0	1
000780	*	1	C	0	0	0	0	0
000810	*	1	C	0	C	0	C	0
000840	*	1	0	0	C	0	0	0
000870	*	1	0	0	0	0	C	0
000900	*	0	1	0	C	C	C	0
000930	*	C	1	0	0	C	C	0
000960	*	0	1	C	0	C	C	0
000990	*	1	C	C	0	C	C	0
001020	*	1	0	0	C	0	0	0
001050	*	1	0	0	0	0	C	0
001080	*	1	0	0	0	C	C	0
001110	*	C	0	1	C	C	C	0
001140	*	1	C	0	C	C	C	0
001170	*	1	C	C	0	C	C	0
001200	*	1	0	0	C	0	0	0
001230	*	1	C	0	0	C	C	0
001260	*	C	0	0	1	C	0	0
001290	*	1	C	0	0	0	0	0

TIME	GATE	SYNOUT	PCOUT	TCLT	HCOUT	XCOUT	YOUT
001320 *	1	0	0	0	0	0	0
001350 *	1	0	0	0	0	0	0
001380 *	1	0	0	0	0	0	0
00141C *	0	0	0	0	1	0	0
001440 *	1	0	0	0	0	0	0
00147C *	1	0	0	0	0	0	0
001500 *	1	0	0	0	0	0	0
001530 *	1	0	0	0	0	0	0
00156C *	0	0	0	0	0	1	0
00159C *	1	0	0	0	0	0	0
001620 *	1	0	0	0	0	0	0
001650 *	1	0	0	0	0	0	0
001680 *	1	0	0	0	0	0	0
001710 *	0	0	0	0	0	0	1
001740 *	1	0	0	0	0	0	0
001770 *	1	0	0	0	0	0	0
00180C *	1	0	0	0	0	0	0
001830 *	1	0	0	0	0	0	0
00186C *	0	1	0	0	0	0	0
001890 *	0	1	0	0	0	0	0
001920 *	0	1	0	0	0	0	0
001950 *	1	0	0	0	0	0	0
001980 *	1	0	0	0	0	0	0
002010 *	1	0	0	0	0	0	0
002040 *	1	0	0	0	0	0	0
00207C *	0	0	1	0	0	0	0
002100 *	1	0	0	0	0	0	0
00213C *	1	0	0	0	0	0	0
002160 *	1	0	0	0	0	0	0
002190 *	1	0	0	0	0	0	0
00222C *	0	0	0	1	0	0	0
002250 *	1	0	0	0	0	0	0
002280 *	1	0	0	0	0	0	0
002310 *	1	0	0	0	0	0	0
002340 *	1	0	0	0	0	0	0
00237C *	0	0	0	0	1	0	0
002400 *	1	0	0	0	0	0	0
002430 *	1	0	0	0	0	0	0
002460 *	1	0	0	0	0	0	0
002490 *	1	0	0	0	0	0	0
00252C *	0	0	0	0	0	1	0
002550 *	1	0	0	0	0	0	0
002580 *	1	0	0	0	0	0	0
002610 *	1	0	0	0	0	0	0

TIME	OFFGATE	SYNOUT	PCOUT	TCOUT	HCOUT	XOUT	YOUT
002640	* 1	0	0	0	0	0	0
002670	* 0	0	0	0	0	0	1
002700	* 1	0	0	0	0	0	0
002730	* 1	0	0	0	0	0	0
002760	* 1	0	0	0	0	0	0
002790	* 1	0	0	0	0	0	0
002820	* 0	1	0	0	0	0	0
002850	* 0	1	0	0	0	0	0
002880	* 0	1	0	0	0	0	0
002910	* 1	0	0	0	0	0	0
002940	* 1	0	0	0	0	0	0
002970	* 1	0	0	0	0	0	0
003000	* 1	0	0	0	0	0	0
003030	* 0	0	1	0	0	0	0
003060	* 1	0	0	0	0	0	0
003090	* 1	0	0	0	0	0	0
003120	* 1	0	0	0	0	0	0
003150	* 1	0	0	0	0	0	0
003180	* 0	0	0	1	0	0	0
003210	* 1	0	0	0	0	0	0
003240	* 1	0	0	0	0	0	0
003270	* 1	0	0	0	0	0	0
003300	* 1	0	0	0	0	0	0
003330	* 0	0	0	0	1	0	0
003360	* 1	0	0	0	0	0	0
003390	* 1	0	0	0	0	0	0
003420	* 1	0	0	0	0	0	0
003450	* 1	0	0	0	0	0	0
003480	* 0	0	0	0	0	1	0
003510	* 1	0	0	0	0	0	0
003540	* 1	0	0	0	0	0	0
003570	* 1	0	0	0	0	0	0
003600	* 1	0	0	0	0	0	0
003630	* 0	0	0	0	0	0	1
003660	* 1	0	0	0	0	0	0
003690	* 1	0	0	0	0	0	0
003720	* 1	0	0	0	0	0	0
003750	* 1	0	0	0	0	0	0
003780	* 0	1	0	0	0	0	0
003810	* 0	1	0	0	0	0	0
003840	* 0	1	0	0	0	0	0
003870	* 1	0	0	0	0	0	0
003900	* 1	0	0	0	0	0	0
003930	* 1	0	0	0	0	0	0

TIME	OFGATE	SYNOUT	PCOUT	TCOUT	HCOUT	XOUT	YOUT
003960	1	0	0	0	0	0	0
003990	0	0	1	0	0	0	0
004020	1	0	0	0	0	0	0
004050	1	0	0	0	0	0	0
004080	1	0	0	0	0	0	0
004110	1	0	0	0	0	0	0
004140	0	0	0	1	0	0	0
004170	1	0	0	0	0	0	0
004200	1	0	0	0	0	0	0
004230	1	0	0	0	0	0	0
004260	1	0	0	0	0	0	0
004290	0	0	0	0	1	0	0
004320	1	0	0	0	0	0	0
004350	1	0	0	0	0	0	0
004380	1	0	0	0	0	0	0
004410	1	0	0	0	0	0	0
004440	0	0	0	0	0	1	0
004470	1	0	0	0	0	0	0
004500	1	0	0	0	0	0	0
004530	1	0	0	0	0	0	0
004560	1	0	0	0	0	0	0
004590	0	0	0	0	0	0	1
004620	1	0	0	0	0	0	0
004650	1	0	0	0	0	0	0
004680	1	0	0	0	0	0	0
004710	1	0	0	0	0	0	0
004740	0	1	0	0	0	0	0
004770	0	1	0	0	0	0	0
004800	0	1	0	0	0	0	0
004830	1	0	0	0	0	0	0
004860	1	0	0	0	0	0	0
004890	1	0	0	0	0	0	0
004920	1	0	0	0	0	0	0
004950	0	0	1	0	0	0	0
004980	1	0	0	0	0	0	0
005010	1	0	0	0	0	0	0
005040	1	0	0	0	0	0	0
005070	1	0	0	0	0	0	0
005100	0	0	0	1	0	0	0
005130	1	0	0	0	0	0	0
005160	1	0	0	0	0	0	0
005190	1	0	0	0	0	0	0
005220	1	0	0	0	0	0	0
005250	0	0	0	0	1	0	0

```
                C
                F   S
      T         F   Y       P       T       H       X       Y
      I         G . N . O . U . T . U . T . U . T . U . T . U . T
      M         A   O       T       T       T       T       T
      E         T   U
                E   T
-------------------------------------------------------------------
 005280 * 1     0   0       0       0       0       0       0
 005310 * 1     0   0       0       0       0       0       0
 005340 * 1     0   0       0       0       0       0       0
 005370 * 1     0   0       0       0       0       0       0
 005400 * 0     0   0       0       0       1       0       0
 005430 * 1     0   0       0       0       0       0       0
 005460 * 1     0   0       0       0       0       0       0
 005490 * 1     0   0       0       0       0       0       0
 005520 * 1     0   0       0       0       0       0       0
 005550 * 0     0   0       0       0       0       0       1
 005580 * 1     0   0       0       0       0       0       0
 005610 * 1     0   0       0       0       0       0       0
 005640 * 1     0   0       0       0       0       0       0
 005670 * 1     0   0       0       0       0       0       0
 005700 * 0     1   0       0       0       0       0       0
 005730 * 0     1   0       0       0       0       0       0
 005760 * 0     1   0       0       0       0       0       0
 005790 * 1     0   0       0       0       0       0       0
 005820 * 1     0   0       0       0       0       0       0
 005850 * 1     0   0       0       0       0       0       0
 005880 * 1     0   0       0       0       0       0       0
 005910 * 0     0   1       0       0       0       0       0
 005940 * 1     0   0       0       0       0       0       0
 005970 * 1     0   0       0       0       0       0       0
 006000 * 1     0   0       0       0       0       0       0

   END OF SIMULATION OUTPUT
/&
AE 09 04 43.25      ET 00 03 08.08
```

APPENDIX C LEAST SQUARE FIT PROGRAM

```
      DIMENSION AA(12,12),Z(12,12),YY(12,12)
      CALL POLCUR (AA,Z,YY, 2,5,12,12,12)
      END


      SUBROUTINE POLCUR (A,Z,Y,M,L, ND,MD,LD)
      DIMENSION A(12,12),AT(12,12),ATA(12,12),ATAINV(12,12),
     1Z(12,12),E7(12,12),Y(12,12),AV(12,12),XX(12),ZZ(12),EE
      REAL*8 TITLE(12),LBLS/8H        /
      REAL*4 LBL(20),XX,ZZ,EE
C**** THIS PROGRAM DETERMINES A POLYNOMIAL LEAST SQUARE FITTED
C
C     GIVEN A SET OF DATA, Z(I),I=1,L
C
C     DETERMINE THE COEFFICIENTS Y(J),J=1,N OF A POLYNOMIAL,
C
C        MINIMIZE  THE ERROR IN THE LOSS FUNCTION,
C
C                  T
C          L=(Z-AY)(Z-AY)
C
C     THE Y(J) ACCOMPLISHING THIS IS
C
C                    -1
C          Y= (AT*A)  *AT*Z
C
C        WHERE
C
C
C
C        AND
C                     1  -TL  +(TL)**2/2-(TL)**3/3  -(TL)**M/M
C                     .   .      .
C                     .   .      .
C                     .   .      .
C          A(I,J)=C   1  -T3  +(T3)**2/2-(T3)**3/3  ...
C                     1  -T2  +(T2)**2/2-(T2)**3/3  ...
C                     1  -T1  +(T1)**2/2-(T1)**3/3  -(T1)**M/M
      KK=11
      N=M+1
      DT=1.0
      READ(5,1)((A(I,J),J=1,N),I=1,L)
    1 FORMAT(3E10.4)
      READ(5,25)(TITLE(I),I=1,12)
   25 FORMAT(6A8,/,6A8)
      READ(5,24) (LBL(I),I=1,20)
   24 FORMAT(20A4)
      DO 2 K=1,KK
C     IF ND=THE NUMBER OF RUNS OF DATA Z(I);THEN THE AVERAGE
C     OF EACH Z(I) IS CALCULATED
      NR=3
      DO 4 II=1,L
      READ(5,4) (AV(NM,II),NM=1,NR)
    4 FORMAT(3E10.4)
      SUM=0.0
      DO 5 JJ=1,NR
      SUM=AV(JJ,II)+SUM
    5 CONTINUE
      AVE=SUM/NR
      Z(II,1)=AVE
    4 CONTINUE
      CALL TRANS(A, L, N,AT,ND,MD)
      CALL PROD ( AT,A, N,L,N ,ATA,ND,MD,LD)
      CALL RECIP (N ,.000001,ATA,ATAINV,KER,MD)
      IF (KER-2) 101,110,101
  110 WRITE(6,111)
  111 FORMAT (5HKER=2)
  101 CALL PROD (ATAINV,AT, N, N, L, C, ND, MD, LD)
      CALL PROD (C,Z, N, L, 1, Y , ND, MD, LD )
      CALL PROD (A,Y, L,N , 1, E7, ND, MD, LD )
      WRITE(6,102)((A(I,J),J=1,N),I=1,L)
  102 FORMAT(//10X,7HA(I,J)=/(2E10.6))
```

```
      WRITE(6,103)((C(I,J),J=1,L),I=1,N)
  103 FORMAT(/1CX,14HDATAINVAT(I,J)=/(4E1C.6))
      WRITE(6,105)(Z(I,1),I=1,L)
  105 FORMAT(/1CX,5HZ(I)=/(1E10.6))
      WRITE(6,104)(Y(I,1)   ,I=1,N)
  104 FORMAT(/1CX,5HY(I)=/(1E10.6))
      WRITE(6,106)(EZ(I,1),I=1,L)
  106 FORMAT(/1CX,6HEZ(I)=/( 1E10.6))
      DO 8 NN=1,L
      XX(NN)=3.0+A(NN,2)
      ZZ(NN)=EZ(NN,1)-30.0
      EE(NN)=EZ(NN,1)-Z(NN,1)
    8 CONTINUE
      IF(K.EQ.1) GO TO 11
      IF(K.LT.11) GO TO 12
      IF(K.EQ.11) GO TO 13
   11 MC=1
      GO TO 14
   12 MC=2
      GO TO 14
   13 MC=3
      GO TO 14
   14 CALL DRAW(6,XX,EE,MC,0,LBL(K),TITLE,1.,.02,3,0,2,0,6,6
    2 CONTINUE
      END


      SUBROUTINE ADD (A,B,N,M,C,ND,MD)
      DIMENSION A(ND,MD),B(ND,MD),C(ND,MD)
      DO 152 I=1,N
      DO 152 J=1,M
  152 C(I,J) = A(I,J) + B(I,J)
      RETURN
      END


      SUBROUTINE SUB (A,B,N,M,C,ND,MD)
      DIMENSION A(ND,MD),B(ND,MD),C(ND,MD)
      DO 152 I=1,N
      DO 152 J=1,M
  152 C(I,J) = A(I,J) - B(I,J)
      RETURN
      END


      SUBROUTINE PROD (A,B,N,M,L,C,ND,MD,LD)
      DIMENSION A(ND,MD),B(MD,LD),C(ND,LD)
      DO 1 I=1,ND
      DO 1 J=1,LD
    1 C(I,J)=0.
      DO 151 I=1,N
      DO 151 J=1,L
      DO 151 K = 1,M
  151 C(I,J) = C(I,J) + A(I,K)*B(K,J)
      RETURN
      END


      SUBROUTINE TRANS(A,N,M,C,ND,MD)
      DIMENSION A(ND,MD),C(MD,ND)
      DO 153 I = 1,N
      DO 153 J=1,M
  153 C(J,I) = A(I,J)
      RETURN
      END


      SUBROUTINE CONST(Q,A,N,M,C,ND,MD)
      DIMENSION A(ND,MD),C(ND,MD)
      IF(Q)11,10,11
   10 DO 100 I=1,N
      DO 100 J=1,M
```

```
100 C(I,J) = 0.0
    RETURN
 11 IF(Q-1.0)13,12,13
 12 DO 120 I=1,N
    DO 120 J=1,M
120 C(I,J) = A(I,J)
    RETURN
 13 IF(Q+1.0)15,14,15
 14 DO 140 I=1,N
    DO 140 J=1,M
140 C(I,J) = -A(I,J)
    RETURN
 15 DO 150 I=1,N
    DO 150 J=1,M
150 C(I,J) = Q*A(I,J)
    RETURN
    END


    SUBROUTINE RECIP(N,EP,A,X,KEP,M)
    DIMENSION A(M,M),X(M,M)
    DO 1 I=1,M
    DO 1 J=1,M
  1 X(I,J)=0.
    DO 2 K=1,N
  2 X(K,K)=1.
 10 DO 34 L=1,N
    KP=0
    Z=0.
    DO 12 K=L,N
    IF(Z.GE.ABS(A(K,L))) GO TO 12
 11 Z=ABS(A(K,L))
    KP=K
 12 CONTINUE
    IF(L.GE.KP) GO TO 20
 13 DO 14 J=L,N
    Z=A(L,J)
    A(L,J)=A(KP,J)
 14 A(KP,J)=Z
    DO 15 J=1,N
    Z=X(L,J)
    X(L,J)=X(KP,J)
 15 X(KP,J)=Z
 20 IF(ABS(A(L,L)).LE.EP) GO TO 50
 30 IF(L.GE.N) GO TO 34
 31 LP1=L+1
    DO 36 K=LP1,N
    IF(A(K,L).EQ.0.) GO TO 36
 32 RATIO=A(K,L)/A(L,L)
    DO 33 J=LP1,N
 33 A(K,J)=A(K,J)-RATIO*A(L,J)
    DO 35 J=1,N
 35 X(K,J)=X(K,J)-RATIO*X(L,J)
 36 CONTINUE
 34 CONTINUE
 40 DO 43 I=1,N
    I1=N+1-I
    DO 43 J=1,N
    S=0.
    IF(I1.GE.N) GO TO 43
 41 IIP1=I1+1
    DO 42 K=IIP1,N
 42 S=S+A(I1,K)*X(K,J)
 43 X(I1,J)=(X(I1,J)-S)/A(I1,I1)
    KEP=1
    RETURN
 50 KEP=2
    RETURN
    END
```

```
      SUBROUTINE MREAD(A,N,M,ND,MD,IREAD)
      SUBROUTINE MREAD(A,N,M,ND,MD,IREAD)
      DIMENSION A(ND,MD),IREAD(10)
      DO 10 I=1,N
```

```
   10 READ(5,20)(A(I,J),J=1,M)
   20 FORMAT(8F10.5)
      RETURN
      END
//GO.SYSIN DD *
1.0          -3.0          4.5
1.0          -2.0          2.0
1.0          -1.0          .5
1.0           0.0          0.0
1.0           1.0          .5
1.0           2.0          2.0
A. SAGERIAN BOX 728, THESIS VCM OUTPUT, 2ND ORD
HORIZ=NEG VOLTS; VERT=DEV FM 2ND ORD APPROX.
+75C+60C+45C+30C+15C 0CC-15C-30C-45C-60C-67C
38.073       37.919       37.880
46.858       46.627       46.628
55.823       55.557       55.552
64.066       64.696       64.672
74.535       74.082       74.029
83.860       83.866       83.785
37.868       37.683       37.720
46.548       46.463       46.421
55.510       55.257       55.374
64.400       64.415       64.446
74.010       73.784       73.774
83.570       83.366       83.390
37.420       37.457       37.420
46.229       46.204       46.116
55.166       55.075       54.997
64.189       64.137       64.030
73.468       73.395       73.271
83.045       82.692       82.792
37.225       37.125       37.095
45.818       45.835       45.731
54.682       54.630       54.529
63.710       63.623       63.515
72.012       72.826       72.698
82.417       82.243       82.078
36.695       36.663       36.567
45.531       45.297       45.144
54.077       54.035       53.901
63.044       62.932       62.770
72.116       72.003       71.817
81.389       81.298       81.089
36.146       36.107       36.000
44.661       44.618       44.528
53.276       53.270       53.096
62.005       62.050       61.867
71.076       71.008       70.821
80.240       80.212       79.989
35.383       35.481       35.305
43.757       43.913       43.715
52.267       52.492       52.176
60.895       61.160       60.767
69.665       69.957       69.523
78.645       78.936       78.486
34.892       34.827       34.726
43.175       43.109       43.008
51.566       51.504       51.400
60.122       60.034       59.864
68.780       68.685       68.511
77.544       77.502       77.310
34.053       34.046       33.970
42.229       42.165       42.090
50.449       50.424       50.272
58.843       58.743       58.619
67.222       67.161       67.064
75.944       75.713       75.618
33.160       33.171       33.039
41.157       41.135       40.990
49.146       49.128       49.000
57.264       57.267       57.105
```

65.530	65.465	65.288
73.633	73.770	73.590
32.790	32.781	32.680
40.620	40.565	40.472
48.520	48.487	48.361
56.590	56.487	56.356
64.640	64.621	64.423
72.838	72.826	72.570

APPENDIX D FIRST ORDER LEAST SQUARE FIT PRINTOUT

```
          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.0
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
37.959320
46.704651
55.657319
64.811325
74.215317
83.836990

          Y(I)=
65.117493
 9.173553

          EZ(I)=
37.596848
46.770401
55.943939
65.117493
74.291031
83.464584


          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.0
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
37.756680
46.477325
55.413651
64.486984
73.856659
83.441986

          Y(I)=
64.805054
 9.132465

          EZ(I)=
37.407669
46.540131
55.672577
64.805054
73.937515
83.069977
```

```
          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
37.432327
46.132983
55.079315
64.118652
73.377991
82.842987

          Y(I)=
64.377197
 9.076504

          EZ(I)=
37.147690
46.224197
55.300690
64.377197
73.453690
82.530197


          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
37.144089
45.794647
54.613647
63.615982
72.811981
82.245987

          Y(I)=
63.879105
 9.015981

          EZ(I)=
36.831177
45.847153
54.863113
63.879105
72.895081
81.911057
```

```
          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.000000
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
36.641647
45.323900
54.004319
62.915314
71.978653
81.258316

          Y(I)=
63.143494
 8.913095

          EZ(I)=
36.404221
45.317307
54.230392
63.143494
72.056586
80.969681


          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.000000
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
36.084320
44.602325
53.213989
62.003983
70.968323
80.146989

          Y(I)=
62.239441
 8.805751

          EZ(I)=
35.822189
44.627945
53.433685
62.239441
71.045181
79.850937
```

```
          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.0
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
35.389648
43.754983
52.311661
60.940659
69.714981
78.489987

          Y(I)=
61.133911
 8.654019

          EZ(I)=
35.171860
43.825882
52.479888
61.133911
69.787918
78.441940


          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.0
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
34.814987
43.097321
51.439990
60.006653
68.658661
77.451996

          Y(I)=
60.182495
 8.525306

          EZ(I)=
34.606583
43.131897
51.657181
60.182495
68.707794
77.233093
```

```
          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
34.022986
42.161316
50.381653
58.734985
67.148987
75.724991

          Y(I)=
58.864685
 8.337896

          EZ(I)=
33.850998
42.188904
50.526779
58.864685
67.202576
75.540466


          A(I,J)=
 1.000000  -3.000000
 1.000000  -2.000000
 1.000000  -1.000000
 1.000000   0.
 1.000000   1.000000
 1.000000   2.000000

          ATAINVAT(I,J)=
 0.095238   0.123809   0.152381   0.180952
 0.209524   0.238095  -0.142857  -0.085714
-0.028571   0.028571   0.085714   0.142857

          Z(I)=
33.123322
41.093994
49.094315
57.211990
65.427658
73.727646

          Y(I)=
57.338882
 8.118293

          EZ(I)=
32.984009
41.102310
49.220581
57.338882
65.457169
73.575455
```

```
          A(I,J)=
 1.000000 -3.000000
 1.000000 -2.000000
 1.000000 -1.000000
 1.000000  0.0
 1.000000  1.000000
 1.000000  2.000000

          ATAINVAT(I,J)=
 0.095238  0.123809  0.152381  0.180952
 0.209524  0.238095 -0.142857 -0.085714
-0.028571  0.028571  0.085714  0.142857

          Z(I)=
32.750320
40.553650
48.455994
56.474319
64.561325
72.744659

          Y(I)=
56.590134
 8.000371

          EZ(I)=
32.589035
40.589401
48.589752
56.590134
64.590500
72.590866

GRAPH TITLED
     A. SAGERIAN BOX 72B, THESIS,VCM OUTPUT, 1ST ORD
     HORIZ=NEG VOLTS; VERT=DEV FM 1ST ORD APPROX.
HAS BEEN PLOTTED.
```

APPENDIX E SECOND ORDER LEAST SQUARE FIT PRINTOUT

```
          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
37.959320
46.704651
55.657318
64.811325
74.215317
83.836990

          Y(I)=
64.822998
 0.284028
 0.220950

          SZ(I)=
37.965179
46.696838
55.649429
64.822998
74.217499
83.932947


          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
37.756989
46.477325
55.413651
64.486984
73.856659
83.441986
```

```
          Y(I)=
 64.516709
  0.240633
  0.216355

          F7(I)=
 37.768387
 46.468140
 55.384232
 64.516709
 73.865509
 83.430695


          A(I,J)=
  1.000000 -3.000000
  4.500000  1.000000
 -2.000000  2.000000
  1.000000 -1.000000
  0.500000  1.000000
  0.0       0.0
  1.000000  1.000000
  0.500000  1.000000
  2.000000  2.000000

          ATA[NVAT(I,I)=
 -0.142857  0.171429  0.342858  0.371429
  0.257143 -0.000001 -0.053571 -0.103571
 -0.100000 -0.042857  0.067857  0.232143
  0.178572 -0.035714 -0.142857 -0.142857
 -0.035714  0.178572

          Y(I)=
 37.432327
 46.182983
 55.079315
 64.118652
 73.377991
 82.842987

          Y(I)=
 64.138107
  0.166200
  0.179403

          F7(I)=
 37.446823
 46.164505
 55.061584
 64.138107
 73.393967
 82.829300


          A(I,J)=
  1.000000 -3.000000
  4.500000  1.000000
 -2.000000  2.000000
  1.000000 -1.000000
  0.500000  1.000000
  0.0       0.0
  1.000000  1.000000
  0.500000  1.000000
  2.000000  2.000000

          ATA[NVAT(I,I)=
 -0.142857  0.171429  0.342858  0.371429
  0.257143 -0.000001 -0.053571 -0.103571
 -0.100000 -0.042857  0.067857  0.232143
  0.178572 -0.035714 -0.142857 -0.142857
 -0.035714  0.178572
```

```
          Z(I)=
37.144989
45.796667
54.613647
63.615982
72.811981
82.245987

          Y(I)=
63.620667
 0.112936
 0.193004

          EZ(I)=
37.154419
45.782609
54.604640
63.620667
72.830536
82.234329


          A(I,J)=
 1.000000  -3.000000
 4.500000   1.000000
-2.000000   2.000000
 1.000000  -1.000000
 0.500000   1.000000
 0.0        0.0
 1.000000   1.000000
 0.500000   1.000000
 2.000000   2.000000

          ATAINVAT(I,J)=
-0.142857   0.171429   0.342858   0.371429
 0.257143  -0.000001  -0.057571  -0.100571
-0.100000  -0.042857   0.057857   0.232143
 0.178572  -0.035714  -0.142857  -0.142857
-0.035714   0.178572

          Z(I)=
36.641647
45.323990
54.004319
62.915314
71.978653
81.258316

          Y(I)=
62.928421
 8.993783
 0.161366

          EZ(I)=
36.673219
45.263580
54.015305
62.928421
72.002869
81.238709
```

```
          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
36.084320
44.602325
53.213989
62.003983
70.968323
80.146989

          Y(I)=
62.015091
 8.889913
 0.168344

          EZ(I)=
36.102875
44.571945
53.209335
62.015091
70.989164
80.131607


          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
35.389649
43.794983
52.311661
60.940659
69.714981
78.689987
```

```
          Y(I)=
60.949310
 8.723280
 0.138519

          F7(I)=
35.402817
43.779800
52.205200
60.949310
69.741837
78.672897


          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
34.814997
43.097321
51.488000
60.006653
68.658641
77.451956

          Y(I)=
60.011536
 8.598440
 0.128294

          F7(I)=
34.820496
43.089218
51.486221
60.011536
68.665100
77.446974


          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572
```

```
          Z(I)=
34.022980
42.161316
50.381653
58.734985
67.148987
75.724991

          Y(I)=
58.723679
 8.390795
 0.105808

          CZ(I)=
34.027435
42.153702
50.395773
58.723679
67.167374
75.716873


          A(I,J)=
 1.000000 -3.000000
 4.500000  1.000000
-2.000000  2.000000
 1.000000 -1.000000
 0.500000  1.000000
 0.0       0.0
 1.000000  1.000000
 0.500000  1.000000
 2.000000  2.000000

          ATAINVAT(I,J)=
-0.142857  0.171429  0.342858  0.371429
 0.257143 -0.000001 -0.053571 -0.103571
-0.100000 -0.042857  0.067857  0.232143
 0.178572 -0.035714 -0.142857 -0.142857
-0.035714  0.178572

          Z(I)=
33.123322
41.093994
49.094315
57.211990
65.427658
73.727646

          Y(I)=
57.219559
 8.163067
 0.089558

          CZ(I)=
33.133362
41.072540
49.101257
57.219559
65.427383
73.724792
```

```
          A(I,J)=
 1.000000  -3.000000
 4.500000   1.000000
-2.000000   2.000000
 1.000000  -1.000000
 0.500000   1.000000
 0.0        0.0
 1.000000   1.000000
 0.500000   1.000000
 2.000000   2.000000

          ATATNVAT(I,J)=
-0.142857   0.171429   0.342858   0.371429
 0.257143  -0.000001  -0.053571  -0.103571
-0.100000  -0.042857   0.067857   0.232143
 0.178572  -0.035714  -0.142857  -0.142857
-0.035714   0.178572

          Z(I)=
32.750320
40.553650
48.455964
56.474319
64.561325
72.744659

          Y(I)=
56.464600
 8.047679
 0.094225

          EZ(I)=
32.746185
40.558080
48.464219
56.464600
64.559174
72.748001

GRAPH TITLED
     A. SACERIAN BOX 728, THESIS VCM OUTPUT, 2ND ORD
     HORIZ=NEG VOLTS; VERT=DEV FM 2ND ORD APPROX.
HAS BEEN PLOTTED.
```

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13. ABSTRACT

This thesis is concerned with the design and construction of a radiosonde utilizing solid state devices and state-of-the-art techniques. The radiosonde is designed with the idea of obtaining data at a ground station in digital form and transmitting this data direct to Weather Central via high speed data links. Pulse modulation is utilized to transmit the data from the radiosonde. The multiplexer (time multiplexing is utilized) is designed using MOS micro technology and a breadboarded simulation is accomplished using discrete MOS integrated circuits. A computer simulation of the actual multiplexer design is performed. The modulator and transmitter are of complete solid state design. Extensive testing of the overall system indicated satisfactory results and show a substantial improvement over the present radiosonde. Modification of ground receiving systems to facilitate proper reception of information from the radiosonde is also discussed.

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14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Solid State						
Pulse Modulation						